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;Supported Devices:

; EFM8UB20F32G

; EFM8UB20F32G

; EFM8UB20F32G

; EFM8UB20F64G

; EFM8UB20F64G

; EFM8UB20F64G

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; ADC0CF Enums (ADC0 Configuration @ 0xBC)

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ADC0CF\_ADLJST\_\_BMASK EQU 004H ; ADC0 Left Justify Select

ADC0CF\_ADLJST\_\_SHIFT EQU 002H ; ADC0 Left Justify Select

ADC0CF\_ADLJST\_\_RIGHT\_JUSTIFIED EQU 000H ; Data in the ADC0H:ADC0L registers is right-

; justified.

ADC0CF\_ADLJST\_\_LEFT\_JUSTIFIED EQU 004H ; Data in the ADC0H:ADC0L registers is left-

; justified.

ADC0CF\_ADSC\_\_FMASK EQU 0F8H ; SAR Clock Divider

ADC0CF\_ADSC\_\_SHIFT EQU 003H ; SAR Clock Divider

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; ADC0CN0 Enums (ADC0 Control @ 0xE8)

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ADC0CN0\_ADCM\_\_FMASK EQU 007H ; Start of Conversion Mode Select

ADC0CN0\_ADCM\_\_SHIFT EQU 000H ; Start of Conversion Mode Select

ADC0CN0\_ADCM\_\_ADBUSY EQU 000H ; ADC0 conversion initiated on write of 1 to ADBUSY.

ADC0CN0\_ADCM\_\_TIMER0 EQU 001H ; ADC0 conversion initiated on overflow of Timer 0.

ADC0CN0\_ADCM\_\_TIMER2 EQU 002H ; ADC0 conversion initiated on overflow of Timer 2.

ADC0CN0\_ADCM\_\_TIMER1 EQU 003H ; ADC0 conversion initiated on overflow of Timer 1.

ADC0CN0\_ADCM\_\_CNVSTR EQU 004H ; ADC0 conversion initiated on rising edge of

; CNVSTR.

ADC0CN0\_ADCM\_\_TIMER3 EQU 005H ; ADC0 conversion initiated on overflow of Timer 3.

ADC0CN0\_ADCM\_\_TIMER4 EQU 006H ; ADC0 conversion initiated on overflow of Timer 4.

ADC0CN0\_ADCM\_\_TIMER5 EQU 007H ; ADC0 conversion initiated on overflow of Timer 5.

ADC0CN0\_ADWINT\_\_BMASK EQU 008H ; Window Compare Interrupt Flag

ADC0CN0\_ADWINT\_\_SHIFT EQU 003H ; Window Compare Interrupt Flag

ADC0CN0\_ADWINT\_\_NOT\_SET EQU 000H ; An ADC window compare event did not occur.

ADC0CN0\_ADWINT\_\_SET EQU 008H ; An ADC window compare event occurred.

ADC0CN0\_ADBUSY\_\_BMASK EQU 010H ; ADC Busy

ADC0CN0\_ADBUSY\_\_SHIFT EQU 004H ; ADC Busy

ADC0CN0\_ADBUSY\_\_NOT\_SET EQU 000H ; An ADC0 conversion is not currently in progress.

ADC0CN0\_ADBUSY\_\_SET EQU 010H ; ADC0 conversion is in progress or start an ADC0

; conversion.

ADC0CN0\_ADINT\_\_BMASK EQU 020H ; Conversion Complete Interrupt Flag

ADC0CN0\_ADINT\_\_SHIFT EQU 005H ; Conversion Complete Interrupt Flag

ADC0CN0\_ADINT\_\_NOT\_SET EQU 000H ; ADC0 has not completed a conversion since the last

; time ADINT was cleared.

ADC0CN0\_ADINT\_\_SET EQU 020H ; ADC0 completed a data conversion.

ADC0CN0\_ADTM\_\_BMASK EQU 040H ; Track Mode

ADC0CN0\_ADTM\_\_SHIFT EQU 006H ; Track Mode

ADC0CN0\_ADTM\_\_TRACK\_NORMAL EQU 000H ; Normal Track Mode. When ADC0 is enabled,

; conversion begins immediately following the start-

; of-conversion signal.

ADC0CN0\_ADTM\_\_TRACK\_DELAYED EQU 040H ; Delayed Track Mode. When ADC0 is enabled,

; conversion begins 3 SAR clock cycles following the

; start-of-conversion signal. The ADC is allowed to

; track during this time. Note that there is not a

; tracking delay when the external conversion start

; (CNVSTR) is used as the start-of-conversion

; source.

ADC0CN0\_ADEN\_\_BMASK EQU 080H ; ADC Enable

ADC0CN0\_ADEN\_\_SHIFT EQU 007H ; ADC Enable

ADC0CN0\_ADEN\_\_DISABLED EQU 000H ; ADC0 Disabled (low-power shutdown).

ADC0CN0\_ADEN\_\_ENABLED EQU 080H ; ADC0 Enabled (active and ready for data

; conversions).

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; ADC0GTH Enums (ADC0 Greater-Than High Byte @ 0xC4)

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ADC0GTH\_ADC0GTH\_\_FMASK EQU 0FFH ; Greater-Than High Byte

ADC0GTH\_ADC0GTH\_\_SHIFT EQU 000H ; Greater-Than High Byte

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; ADC0GTL Enums (ADC0 Greater-Than Low Byte @ 0xC3)

;------------------------------------------------------------------------------

ADC0GTL\_ADC0GTL\_\_FMASK EQU 0FFH ; Greater-Than Low Byte

ADC0GTL\_ADC0GTL\_\_SHIFT EQU 000H ; Greater-Than Low Byte

;------------------------------------------------------------------------------

; ADC0H Enums (ADC0 Data Word High Byte @ 0xBE)

;------------------------------------------------------------------------------

ADC0H\_ADC0H\_\_FMASK EQU 0FFH ; Data Word High Byte

ADC0H\_ADC0H\_\_SHIFT EQU 000H ; Data Word High Byte

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; ADC0L Enums (ADC0 Data Word Low Byte @ 0xBD)

;------------------------------------------------------------------------------

ADC0L\_ADC0L\_\_FMASK EQU 0FFH ; Data Word Low Byte

ADC0L\_ADC0L\_\_SHIFT EQU 000H ; Data Word Low Byte

;------------------------------------------------------------------------------

; ADC0LTH Enums (ADC0 Less-Than High Byte @ 0xC6)

;------------------------------------------------------------------------------

ADC0LTH\_ADC0LTH\_\_FMASK EQU 0FFH ; Less-Than High Byte

ADC0LTH\_ADC0LTH\_\_SHIFT EQU 000H ; Less-Than High Byte

;------------------------------------------------------------------------------

; ADC0LTL Enums (ADC0 Less-Than Low Byte @ 0xC5)

;------------------------------------------------------------------------------

ADC0LTL\_ADC0LTL\_\_FMASK EQU 0FFH ; Less-Than Low Byte

ADC0LTL\_ADC0LTL\_\_SHIFT EQU 000H ; Less-Than Low Byte

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; AMX0N Enums (AMUX0 Negative Multiplexer Selection @ 0xBA)

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AMX0N\_AMX0N\_\_FMASK EQU 03FH ; AMUX0 Negative Input Selection

AMX0N\_AMX0N\_\_SHIFT EQU 000H ; AMUX0 Negative Input Selection

AMX0N\_AMX0N\_\_ADC0N0 EQU 000H ; Select ADC0N.0.

AMX0N\_AMX0N\_\_ADC0N1 EQU 001H ; Select ADC0N.1.

AMX0N\_AMX0N\_\_ADC0N2 EQU 002H ; Select ADC0N.2.

AMX0N\_AMX0N\_\_ADC0N3 EQU 003H ; Select ADC0N.3.

AMX0N\_AMX0N\_\_ADC0N4 EQU 004H ; Select ADC0N.4.

AMX0N\_AMX0N\_\_ADC0N5 EQU 005H ; Select ADC0N.5.

AMX0N\_AMX0N\_\_ADC0N6 EQU 006H ; Select ADC0N.6.

AMX0N\_AMX0N\_\_ADC0N7 EQU 007H ; Select ADC0N.7.

AMX0N\_AMX0N\_\_ADC0N8 EQU 008H ; Select ADC0N.8.

AMX0N\_AMX0N\_\_ADC0N9 EQU 009H ; Select ADC0N.9.

AMX0N\_AMX0N\_\_ADC0N10 EQU 00AH ; Select ADC0N.10.

AMX0N\_AMX0N\_\_ADC0N11 EQU 00BH ; Select ADC0N.11.

AMX0N\_AMX0N\_\_ADC0N12 EQU 00CH ; Select ADC0N.12.

AMX0N\_AMX0N\_\_ADC0N13 EQU 00DH ; Select ADC0N.13.

AMX0N\_AMX0N\_\_ADC0N14 EQU 00EH ; Select ADC0N.14.

AMX0N\_AMX0N\_\_ADC0N15 EQU 00FH ; Select ADC0N.15.

AMX0N\_AMX0N\_\_ADC0N16 EQU 010H ; Select ADC0N.16.

AMX0N\_AMX0N\_\_ADC0N17 EQU 011H ; Select ADC0N.17.

AMX0N\_AMX0N\_\_ADC0N18 EQU 012H ; Select ADC0N.18.

AMX0N\_AMX0N\_\_ADC0N19 EQU 013H ; Select ADC0N.19.

AMX0N\_AMX0N\_\_ADC0N20 EQU 014H ; Select ADC0N.20.

AMX0N\_AMX0N\_\_ADC0N21 EQU 015H ; Select ADC0N.21.

AMX0N\_AMX0N\_\_ADC0N22 EQU 016H ; Select ADC0N.22.

AMX0N\_AMX0N\_\_ADC0N23 EQU 017H ; Select ADC0N.23.

AMX0N\_AMX0N\_\_ADC0N24 EQU 018H ; Select ADC0N.24.

AMX0N\_AMX0N\_\_ADC0N25 EQU 019H ; Select ADC0N.25.

AMX0N\_AMX0N\_\_ADC0N26 EQU 01AH ; Select ADC0N.26.

AMX0N\_AMX0N\_\_ADC0N27 EQU 01BH ; Select ADC0N.27.

AMX0N\_AMX0N\_\_ADC0N28 EQU 01CH ; Select ADC0N.28.

AMX0N\_AMX0N\_\_ADC0N29 EQU 01DH ; Select ADC0N.29.

AMX0N\_AMX0N\_\_VREF EQU 01EH ; Internal Voltage Reference.

AMX0N\_AMX0N\_\_GND EQU 01FH ; Ground (single-ended mode).

AMX0N\_AMX0N\_\_ADC0N32 EQU 020H ; Select ADC0N.32.

AMX0N\_AMX0N\_\_ADC0N33 EQU 021H ; Select ADC0N.33.

AMX0N\_AMX0N\_\_ADC0N34 EQU 022H ; Select ADC0N.34.

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; AMX0P Enums (AMUX0 Positive Multiplexer Selection @ 0xBB)

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AMX0P\_AMX0P\_\_FMASK EQU 03FH ; AMUX0 Positive Input Selection

AMX0P\_AMX0P\_\_SHIFT EQU 000H ; AMUX0 Positive Input Selection

AMX0P\_AMX0P\_\_ADC0P0 EQU 000H ; Select ADC0P.0.

AMX0P\_AMX0P\_\_ADC0P1 EQU 001H ; Select ADC0P.1.

AMX0P\_AMX0P\_\_ADC0P2 EQU 002H ; Select ADC0P.2.

AMX0P\_AMX0P\_\_ADC0P3 EQU 003H ; Select ADC0P.3.

AMX0P\_AMX0P\_\_ADC0P4 EQU 004H ; Select ADC0P.4.

AMX0P\_AMX0P\_\_ADC0P5 EQU 005H ; Select ADC0P.5.

AMX0P\_AMX0P\_\_ADC0P6 EQU 006H ; Select ADC0P.6.

AMX0P\_AMX0P\_\_ADC0P7 EQU 007H ; Select ADC0P.7.

AMX0P\_AMX0P\_\_ADC0P8 EQU 008H ; Select ADC0P.8.

AMX0P\_AMX0P\_\_ADC0P9 EQU 009H ; Select ADC0P.9.

AMX0P\_AMX0P\_\_ADC0P10 EQU 00AH ; Select ADC0P.10.

AMX0P\_AMX0P\_\_ADC0P11 EQU 00BH ; Select ADC0P.11.

AMX0P\_AMX0P\_\_ADC0P12 EQU 00CH ; Select ADC0P.12.

AMX0P\_AMX0P\_\_ADC0P13 EQU 00DH ; Select ADC0P.13.

AMX0P\_AMX0P\_\_ADC0P14 EQU 00EH ; Select ADC0P.14.

AMX0P\_AMX0P\_\_ADC0P15 EQU 00FH ; Select ADC0P.15.

AMX0P\_AMX0P\_\_ADC0P16 EQU 010H ; Select ADC0P.16.

AMX0P\_AMX0P\_\_ADC0P17 EQU 011H ; Select ADC0P.17.

AMX0P\_AMX0P\_\_ADC0P18 EQU 012H ; Select ADC0P.18.

AMX0P\_AMX0P\_\_ADC0P19 EQU 013H ; Select ADC0P.19.

AMX0P\_AMX0P\_\_ADC0P20 EQU 014H ; Select ADC0P.20.

AMX0P\_AMX0P\_\_ADC0P21 EQU 015H ; Select ADC0P.21.

AMX0P\_AMX0P\_\_ADC0P22 EQU 016H ; Select ADC0P.22.

AMX0P\_AMX0P\_\_ADC0P23 EQU 017H ; Select ADC0P.23.

AMX0P\_AMX0P\_\_ADC0P24 EQU 018H ; Select ADC0P.24.

AMX0P\_AMX0P\_\_ADC0P25 EQU 019H ; Select ADC0P.25.

AMX0P\_AMX0P\_\_ADC0P26 EQU 01AH ; Select ADC0P.26.

AMX0P\_AMX0P\_\_ADC0P27 EQU 01BH ; Select ADC0P.27.

AMX0P\_AMX0P\_\_ADC0P28 EQU 01CH ; Select ADC0P.28.

AMX0P\_AMX0P\_\_ADC0P29 EQU 01DH ; Select ADC0P.29.

AMX0P\_AMX0P\_\_TEMP EQU 01EH ; Temperature sensor.

AMX0P\_AMX0P\_\_VDD EQU 01FH ; VDD Supply Voltage.

AMX0P\_AMX0P\_\_ADC0P32 EQU 020H ; Select ADC0P.32.

AMX0P\_AMX0P\_\_ADC0P33 EQU 021H ; Select ADC0P.33.

AMX0P\_AMX0P\_\_ADC0P34 EQU 022H ; Select ADC0P.34.

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; ACC Enums (Accumulator @ 0xE0)

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ACC\_ACC\_\_FMASK EQU 0FFH ; Accumulator

ACC\_ACC\_\_SHIFT EQU 000H ; Accumulator

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; B Enums (B Register @ 0xF0)

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B\_B\_\_FMASK EQU 0FFH ; B Register

B\_B\_\_SHIFT EQU 000H ; B Register

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; DPH Enums (Data Pointer High @ 0x83)

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DPH\_DPH\_\_FMASK EQU 0FFH ; Data Pointer High

DPH\_DPH\_\_SHIFT EQU 000H ; Data Pointer High

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; DPL Enums (Data Pointer Low @ 0x82)

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DPL\_DPL\_\_FMASK EQU 0FFH ; Data Pointer Low

DPL\_DPL\_\_SHIFT EQU 000H ; Data Pointer Low

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; PFE0CN Enums (Prefetch Engine Control @ 0xAF)

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PFE0CN\_FLBWE\_\_BMASK EQU 001H ; Flash Block Write Enable

PFE0CN\_FLBWE\_\_SHIFT EQU 000H ; Flash Block Write Enable

PFE0CN\_FLBWE\_\_BLOCK\_WRITE\_DISABLED EQU 000H ; Each byte of a firmware flash write is written

; individually.

PFE0CN\_FLBWE\_\_BLOCK\_WRITE\_ENABLED EQU 001H ; Flash bytes are written in groups of two.

PFE0CN\_PFEN\_\_BMASK EQU 020H ; Prefetch Enable

PFE0CN\_PFEN\_\_SHIFT EQU 005H ; Prefetch Enable

PFE0CN\_PFEN\_\_DISABLED EQU 000H ; Disable the prefetch engine (SYSCLK < 25 MHz).

PFE0CN\_PFEN\_\_ENABLED EQU 020H ; Enable the prefetch engine (SYSCLK > 25 MHz).

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; PSW Enums (Program Status Word @ 0xD0)

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PSW\_PARITY\_\_BMASK EQU 001H ; Parity Flag

PSW\_PARITY\_\_SHIFT EQU 000H ; Parity Flag

PSW\_PARITY\_\_NOT\_SET EQU 000H ; The sum of the 8 bits in the accumulator is even.

PSW\_PARITY\_\_SET EQU 001H ; The sum of the 8 bits in the accumulator is odd.

PSW\_F1\_\_BMASK EQU 002H ; User Flag 1

PSW\_F1\_\_SHIFT EQU 001H ; User Flag 1

PSW\_F1\_\_NOT\_SET EQU 000H ; Flag is not set.

PSW\_F1\_\_SET EQU 002H ; Flag is set.

PSW\_OV\_\_BMASK EQU 004H ; Overflow Flag

PSW\_OV\_\_SHIFT EQU 002H ; Overflow Flag

PSW\_OV\_\_NOT\_SET EQU 000H ; An overflow did not occur.

PSW\_OV\_\_SET EQU 004H ; An overflow occurred.

PSW\_RS\_\_FMASK EQU 018H ; Register Bank Select

PSW\_RS\_\_SHIFT EQU 003H ; Register Bank Select

PSW\_RS\_\_BANK0 EQU 000H ; Bank 0, Addresses 0x00-0x07

PSW\_RS\_\_BANK1 EQU 008H ; Bank 1, Addresses 0x08-0x0F

PSW\_RS\_\_BANK2 EQU 010H ; Bank 2, Addresses 0x10-0x17

PSW\_RS\_\_BANK3 EQU 018H ; Bank 3, Addresses 0x18-0x1F

PSW\_F0\_\_BMASK EQU 020H ; User Flag 0

PSW\_F0\_\_SHIFT EQU 005H ; User Flag 0

PSW\_F0\_\_NOT\_SET EQU 000H ; Flag is not set.

PSW\_F0\_\_SET EQU 020H ; Flag is set.

PSW\_AC\_\_BMASK EQU 040H ; Auxiliary Carry Flag

PSW\_AC\_\_SHIFT EQU 006H ; Auxiliary Carry Flag

PSW\_AC\_\_NOT\_SET EQU 000H ; A carry into (addition) or borrow from

; (subtraction) the high order nibble did not occur.

PSW\_AC\_\_SET EQU 040H ; A carry into (addition) or borrow from

; (subtraction) the high order nibble occurred.

PSW\_CY\_\_BMASK EQU 080H ; Carry Flag

PSW\_CY\_\_SHIFT EQU 007H ; Carry Flag

PSW\_CY\_\_NOT\_SET EQU 000H ; A carry (addition) or borrow (subtraction) did not

; occur.

PSW\_CY\_\_SET EQU 080H ; A carry (addition) or borrow (subtraction)

; occurred.

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; SP Enums (Stack Pointer @ 0x81)

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SP\_SP\_\_FMASK EQU 0FFH ; Stack Pointer

SP\_SP\_\_SHIFT EQU 000H ; Stack Pointer

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; CLKSEL Enums (Clock Select @ 0xA9)

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CLKSEL\_CLKSL\_\_FMASK EQU 007H ; System Clock Source Select Bits

CLKSEL\_CLKSL\_\_SHIFT EQU 000H ; System Clock Source Select Bits

CLKSEL\_CLKSL\_\_DIVIDED\_HFOSC\_DIV\_4 EQU 000H ; Clock (SYSCLK) derived from the Internal High-

; Frequency Oscillator / 4 and scaled per the IFCN

; bits in register OSCICN.

CLKSEL\_CLKSL\_\_EXTOSC EQU 001H ; Clock (SYSCLK) derived from the External

; Oscillator circuit.

CLKSEL\_CLKSL\_\_HFOSC\_DIV\_2 EQU 002H ; Clock (SYSCLK) derived from the Internal High-

; Frequency Oscillator / 2.

CLKSEL\_CLKSL\_\_HFOSC EQU 003H ; Clock (SYSCLK) derived from the Internal High-

; Frequency Oscillator.

CLKSEL\_CLKSL\_\_LFOSC EQU 004H ; Clock (SYSCLK) derived from the Internal Low-

; Frequency Oscillator and scaled per the OSCLD bits

; in register OSCLCN.

CLKSEL\_OUTCLK\_\_BMASK EQU 008H ; Crossbar Clock Out Select

CLKSEL\_OUTCLK\_\_SHIFT EQU 003H ; Crossbar Clock Out Select

CLKSEL\_OUTCLK\_\_SYSCLK EQU 000H ; Enabling the Crossbar SYSCLK signal outputs

; SYSCLK.

CLKSEL\_OUTCLK\_\_SYSCLK\_SYNC\_IO EQU 008H ; Enabling the Crossbar SYSCLK signal outputs SYSCLK

; synchronized with the Port I/O.

CLKSEL\_USBCLK\_\_FMASK EQU 070H ; USB Clock Source Select Bits

CLKSEL\_USBCLK\_\_SHIFT EQU 004H ; USB Clock Source Select Bits

CLKSEL\_USBCLK\_\_HFOSC EQU 000H ; USB clock (USBCLK) derived from the Internal High-

; Frequency Oscillator.

CLKSEL\_USBCLK\_\_HFOSC\_DIV\_8 EQU 010H ; USB clock (USBCLK) derived from the Internal High-

; Frequency Oscillator / 8.

CLKSEL\_USBCLK\_\_EXTOSC EQU 020H ; USB clock (USBCLK) derived from the External

; Oscillator.

CLKSEL\_USBCLK\_\_EXTOSC\_DIV\_2 EQU 030H ; USB clock (USBCLK) derived from the External

; Oscillator / 2.

CLKSEL\_USBCLK\_\_EXTOSC\_DIV\_3 EQU 040H ; USB clock (USBCLK) derived from the External

; Oscillator / 3.

CLKSEL\_USBCLK\_\_EXTOSC\_DIV\_4 EQU 050H ; USB clock (USBCLK) derived from the External

; Oscillator / 4.

CLKSEL\_USBCLK\_\_LFOSC EQU 060H ; USB clock (USBCLK) derived from the Internal Low-

; Frequency Oscillator.

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; CMP0CN0 Enums (Comparator 0 Control 0 @ 0x9B)

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CMP0CN0\_CPHYN\_\_FMASK EQU 003H ; Comparator Negative Hysteresis Control

CMP0CN0\_CPHYN\_\_SHIFT EQU 000H ; Comparator Negative Hysteresis Control

CMP0CN0\_CPHYN\_\_DISABLED EQU 000H ; Negative Hysteresis disabled.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE1 EQU 001H ; Negative Hysteresis = Hysteresis 1.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE2 EQU 002H ; Negative Hysteresis = Hysteresis 2.

CMP0CN0\_CPHYN\_\_ENABLED\_MODE3 EQU 003H ; Negative Hysteresis = Hysteresis 3 (Maximum).

CMP0CN0\_CPHYP\_\_FMASK EQU 00CH ; Comparator Positive Hysteresis Control

CMP0CN0\_CPHYP\_\_SHIFT EQU 002H ; Comparator Positive Hysteresis Control

CMP0CN0\_CPHYP\_\_DISABLED EQU 000H ; Positive Hysteresis disabled.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE1 EQU 004H ; Positive Hysteresis = Hysteresis 1.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE2 EQU 008H ; Positive Hysteresis = Hysteresis 2.

CMP0CN0\_CPHYP\_\_ENABLED\_MODE3 EQU 00CH ; Positive Hysteresis = Hysteresis 3 (Maximum).

CMP0CN0\_CPFIF\_\_BMASK EQU 010H ; Comparator Falling-Edge Flag

CMP0CN0\_CPFIF\_\_SHIFT EQU 004H ; Comparator Falling-Edge Flag

CMP0CN0\_CPFIF\_\_NOT\_SET EQU 000H ; No comparator falling edge has occurred since this

; flag was last cleared.

CMP0CN0\_CPFIF\_\_FALLING\_EDGE EQU 010H ; Comparator falling edge has occurred.

CMP0CN0\_CPRIF\_\_BMASK EQU 020H ; Comparator Rising-Edge Flag

CMP0CN0\_CPRIF\_\_SHIFT EQU 005H ; Comparator Rising-Edge Flag

CMP0CN0\_CPRIF\_\_NOT\_SET EQU 000H ; No comparator rising edge has occurred since this

; flag was last cleared.

CMP0CN0\_CPRIF\_\_RISING\_EDGE EQU 020H ; Comparator rising edge has occurred.

CMP0CN0\_CPOUT\_\_BMASK EQU 040H ; Comparator Output State Flag

CMP0CN0\_CPOUT\_\_SHIFT EQU 006H ; Comparator Output State Flag

CMP0CN0\_CPOUT\_\_POS\_LESS\_THAN\_NEG EQU 000H ; Voltage on CP0P < CP0N.

CMP0CN0\_CPOUT\_\_POS\_GREATER\_THAN\_NEG EQU 040H ; Voltage on CP0P > CP0N.

CMP0CN0\_CPEN\_\_BMASK EQU 080H ; Comparator Enable

CMP0CN0\_CPEN\_\_SHIFT EQU 007H ; Comparator Enable

CMP0CN0\_CPEN\_\_DISABLED EQU 000H ; Comparator disabled.

CMP0CN0\_CPEN\_\_ENABLED EQU 080H ; Comparator enabled.

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; CMP0MD Enums (Comparator 0 Mode @ 0x9D)

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CMP0MD\_CPMD\_\_FMASK EQU 003H ; Comparator Mode Select

CMP0MD\_CPMD\_\_SHIFT EQU 000H ; Comparator Mode Select

CMP0MD\_CPMD\_\_MODE0 EQU 000H ; Mode 0 (Fastest Response Time, Highest Power

; Consumption)

CMP0MD\_CPMD\_\_MODE1 EQU 001H ; Mode 1

CMP0MD\_CPMD\_\_MODE2 EQU 002H ; Mode 2

CMP0MD\_CPMD\_\_MODE3 EQU 003H ; Mode 3 (Slowest Response Time, Lowest Power

; Consumption)

CMP0MD\_CPFIE\_\_BMASK EQU 010H ; Comparator Falling-Edge Interrupt Enable

CMP0MD\_CPFIE\_\_SHIFT EQU 004H ; Comparator Falling-Edge Interrupt Enable

CMP0MD\_CPFIE\_\_FALL\_INT\_DISABLED EQU 000H ; Comparator falling-edge interrupt disabled.

CMP0MD\_CPFIE\_\_FALL\_INT\_ENABLED EQU 010H ; Comparator falling-edge interrupt enabled.

CMP0MD\_CPRIE\_\_BMASK EQU 020H ; Comparator Rising-Edge Interrupt Enable

CMP0MD\_CPRIE\_\_SHIFT EQU 005H ; Comparator Rising-Edge Interrupt Enable

CMP0MD\_CPRIE\_\_RISE\_INT\_DISABLED EQU 000H ; Comparator rising-edge interrupt disabled.

CMP0MD\_CPRIE\_\_RISE\_INT\_ENABLED EQU 020H ; Comparator rising-edge interrupt enabled.

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; CMP0MX Enums (Comparator 0 Multiplexer Selection @ 0x9F)

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CMP0MX\_CMXP\_\_FMASK EQU 007H ; Comparator Positive Input MUX Selection

CMP0MX\_CMXP\_\_SHIFT EQU 000H ; Comparator Positive Input MUX Selection

CMP0MX\_CMXP\_\_CMP0P0 EQU 000H ; External pin CMP0P.0.

CMP0MX\_CMXP\_\_CMP0P1 EQU 001H ; External pin CMP0P.1.

CMP0MX\_CMXP\_\_CMP0P2 EQU 002H ; External pin CMP0P.2.

CMP0MX\_CMXP\_\_CMP0P3 EQU 003H ; External pin CMP0P.3.

CMP0MX\_CMXP\_\_CMP0P4 EQU 004H ; External pin CMP0P.4.

CMP0MX\_CMXN\_\_FMASK EQU 070H ; Comparator Negative Input MUX Selection

CMP0MX\_CMXN\_\_SHIFT EQU 004H ; Comparator Negative Input MUX Selection

CMP0MX\_CMXN\_\_CMP0N0 EQU 000H ; External pin CMP0N.0.

CMP0MX\_CMXN\_\_CMP0N1 EQU 010H ; External pin CMP0N.1.

CMP0MX\_CMXN\_\_CMP0N2 EQU 020H ; External pin CMP0N.2.

CMP0MX\_CMXN\_\_CMP0N3 EQU 030H ; External pin CMP0N.3.

CMP0MX\_CMXN\_\_CMP0N4 EQU 040H ; External pin CMP0N.4.

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; CMP1CN0 Enums (Comparator 1 Control 0 @ 0x9A)

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CMP1CN0\_CPHYN\_\_FMASK EQU 003H ; Comparator Negative Hysteresis Control

CMP1CN0\_CPHYN\_\_SHIFT EQU 000H ; Comparator Negative Hysteresis Control

CMP1CN0\_CPHYN\_\_DISABLED EQU 000H ; Negative Hysteresis disabled.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE1 EQU 001H ; Negative Hysteresis = Hysteresis 1.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE2 EQU 002H ; Negative Hysteresis = Hysteresis 2.

CMP1CN0\_CPHYN\_\_ENABLED\_MODE3 EQU 003H ; Negative Hysteresis = Hysteresis 3 (Maximum).

CMP1CN0\_CPHYP\_\_FMASK EQU 00CH ; Comparator Positive Hysteresis Control

CMP1CN0\_CPHYP\_\_SHIFT EQU 002H ; Comparator Positive Hysteresis Control

CMP1CN0\_CPHYP\_\_DISABLED EQU 000H ; Positive Hysteresis disabled.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE1 EQU 004H ; Positive Hysteresis = Hysteresis 1.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE2 EQU 008H ; Positive Hysteresis = Hysteresis 2.

CMP1CN0\_CPHYP\_\_ENABLED\_MODE3 EQU 00CH ; Positive Hysteresis = Hysteresis 3 (Maximum).

CMP1CN0\_CPFIF\_\_BMASK EQU 010H ; Comparator Falling-Edge Flag

CMP1CN0\_CPFIF\_\_SHIFT EQU 004H ; Comparator Falling-Edge Flag

CMP1CN0\_CPFIF\_\_NOT\_SET EQU 000H ; No comparator falling edge has occurred since this

; flag was last cleared.

CMP1CN0\_CPFIF\_\_FALLING\_EDGE EQU 010H ; Comparator falling edge has occurred.

CMP1CN0\_CPRIF\_\_BMASK EQU 020H ; Comparator Rising-Edge Flag

CMP1CN0\_CPRIF\_\_SHIFT EQU 005H ; Comparator Rising-Edge Flag

CMP1CN0\_CPRIF\_\_NOT\_SET EQU 000H ; No comparator rising edge has occurred since this

; flag was last cleared.

CMP1CN0\_CPRIF\_\_RISING\_EDGE EQU 020H ; Comparator rising edge has occurred.

CMP1CN0\_CPOUT\_\_BMASK EQU 040H ; Comparator Output State Flag

CMP1CN0\_CPOUT\_\_SHIFT EQU 006H ; Comparator Output State Flag

CMP1CN0\_CPOUT\_\_POS\_LESS\_THAN\_NEG EQU 000H ; Voltage on CP1P < CP1N.

CMP1CN0\_CPOUT\_\_POS\_GREATER\_THAN\_NEG EQU 040H ; Voltage on CP1P > CP1N.

CMP1CN0\_CPEN\_\_BMASK EQU 080H ; Comparator Enable

CMP1CN0\_CPEN\_\_SHIFT EQU 007H ; Comparator Enable

CMP1CN0\_CPEN\_\_DISABLED EQU 000H ; Comparator disabled.

CMP1CN0\_CPEN\_\_ENABLED EQU 080H ; Comparator enabled.

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; CMP1MD Enums (Comparator 1 Mode @ 0x9C)

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CMP1MD\_CPMD\_\_FMASK EQU 003H ; Comparator Mode Select

CMP1MD\_CPMD\_\_SHIFT EQU 000H ; Comparator Mode Select

CMP1MD\_CPMD\_\_MODE0 EQU 000H ; Mode 0 (Fastest Response Time, Highest Power

; Consumption)

CMP1MD\_CPMD\_\_MODE1 EQU 001H ; Mode 1

CMP1MD\_CPMD\_\_MODE2 EQU 002H ; Mode 2

CMP1MD\_CPMD\_\_MODE3 EQU 003H ; Mode 3 (Slowest Response Time, Lowest Power

; Consumption)

CMP1MD\_CPFIE\_\_BMASK EQU 010H ; Comparator Falling-Edge Interrupt Enable

CMP1MD\_CPFIE\_\_SHIFT EQU 004H ; Comparator Falling-Edge Interrupt Enable

CMP1MD\_CPFIE\_\_FALL\_INT\_DISABLED EQU 000H ; Comparator falling-edge interrupt disabled.

CMP1MD\_CPFIE\_\_FALL\_INT\_ENABLED EQU 010H ; Comparator falling-edge interrupt enabled.

CMP1MD\_CPRIE\_\_BMASK EQU 020H ; Comparator Rising-Edge Interrupt Enable

CMP1MD\_CPRIE\_\_SHIFT EQU 005H ; Comparator Rising-Edge Interrupt Enable

CMP1MD\_CPRIE\_\_RISE\_INT\_DISABLED EQU 000H ; Comparator rising-edge interrupt disabled.

CMP1MD\_CPRIE\_\_RISE\_INT\_ENABLED EQU 020H ; Comparator rising-edge interrupt enabled.

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; CMP1MX Enums (Comparator 1 Multiplexer Selection @ 0x9E)

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CMP1MX\_CMXP\_\_FMASK EQU 007H ; Comparator Positive Input MUX Selection

CMP1MX\_CMXP\_\_SHIFT EQU 000H ; Comparator Positive Input MUX Selection

CMP1MX\_CMXP\_\_CMP1P0 EQU 000H ; External pin CMP1P.0.

CMP1MX\_CMXP\_\_CMP1P1 EQU 001H ; External pin CMP1P.1.

CMP1MX\_CMXP\_\_CMP1P2 EQU 002H ; External pin CMP1P.2.

CMP1MX\_CMXP\_\_CMP1P3 EQU 003H ; External pin CMP1P.3.

CMP1MX\_CMXP\_\_CMP1P4 EQU 004H ; External pin CMP1P.4.

CMP1MX\_CMXN\_\_FMASK EQU 070H ; Comparator Negative Input MUX Selection

CMP1MX\_CMXN\_\_SHIFT EQU 004H ; Comparator Negative Input MUX Selection

CMP1MX\_CMXN\_\_CMP1N0 EQU 000H ; External pin CMP1N.0.

CMP1MX\_CMXN\_\_CMP1N1 EQU 010H ; External pin CMP1N.1.

CMP1MX\_CMXN\_\_CMP1N2 EQU 020H ; External pin CMP1N.2.

CMP1MX\_CMXN\_\_CMP1N3 EQU 030H ; External pin CMP1N.3.

CMP1MX\_CMXN\_\_CMP1N4 EQU 040H ; External pin CMP1N.4.

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; IT01CF Enums (INT0/INT1 Configuration @ 0xE4)

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IT01CF\_IN0SL\_\_FMASK EQU 007H ; INT0 Port Pin Selection

IT01CF\_IN0SL\_\_SHIFT EQU 000H ; INT0 Port Pin Selection

IT01CF\_IN0SL\_\_P0\_0 EQU 000H ; Select P0.0.

IT01CF\_IN0SL\_\_P0\_1 EQU 001H ; Select P0.1.

IT01CF\_IN0SL\_\_P0\_2 EQU 002H ; Select P0.2.

IT01CF\_IN0SL\_\_P0\_3 EQU 003H ; Select P0.3.

IT01CF\_IN0SL\_\_P0\_4 EQU 004H ; Select P0.4.

IT01CF\_IN0SL\_\_P0\_5 EQU 005H ; Select P0.5.

IT01CF\_IN0SL\_\_P0\_6 EQU 006H ; Select P0.6.

IT01CF\_IN0SL\_\_P0\_7 EQU 007H ; Select P0.7.

IT01CF\_IN0PL\_\_BMASK EQU 008H ; INT0 Polarity

IT01CF\_IN0PL\_\_SHIFT EQU 003H ; INT0 Polarity

IT01CF\_IN0PL\_\_ACTIVE\_LOW EQU 000H ; INT0 input is active low.

IT01CF\_IN0PL\_\_ACTIVE\_HIGH EQU 008H ; INT0 input is active high.

IT01CF\_IN1SL\_\_FMASK EQU 070H ; INT1 Port Pin Selection

IT01CF\_IN1SL\_\_SHIFT EQU 004H ; INT1 Port Pin Selection

IT01CF\_IN1SL\_\_P0\_0 EQU 000H ; Select P0.0.

IT01CF\_IN1SL\_\_P0\_1 EQU 010H ; Select P0.1.

IT01CF\_IN1SL\_\_P0\_2 EQU 020H ; Select P0.2.

IT01CF\_IN1SL\_\_P0\_3 EQU 030H ; Select P0.3.

IT01CF\_IN1SL\_\_P0\_4 EQU 040H ; Select P0.4.

IT01CF\_IN1SL\_\_P0\_5 EQU 050H ; Select P0.5.

IT01CF\_IN1SL\_\_P0\_6 EQU 060H ; Select P0.6.

IT01CF\_IN1SL\_\_P0\_7 EQU 070H ; Select P0.7.

IT01CF\_IN1PL\_\_BMASK EQU 080H ; INT1 Polarity

IT01CF\_IN1PL\_\_SHIFT EQU 007H ; INT1 Polarity

IT01CF\_IN1PL\_\_ACTIVE\_LOW EQU 000H ; INT1 input is active low.

IT01CF\_IN1PL\_\_ACTIVE\_HIGH EQU 080H ; INT1 input is active high.

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; XOSC0CN Enums (External Oscillator Control @ 0xB1)

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XOSC0CN\_XFCN\_\_FMASK EQU 007H ; External Oscillator Frequency Control

XOSC0CN\_XFCN\_\_SHIFT EQU 000H ; External Oscillator Frequency Control

XOSC0CN\_XFCN\_\_MODE0 EQU 000H ; Select external oscillator mode 0: Crystal

; frequency <= 20 kHz, RC/C frequency <= 25 kHz, C

; mode K factor = 0.87.

XOSC0CN\_XFCN\_\_MODE1 EQU 001H ; Select external oscillator mode 1: 20 kHz <

; Crystal frequency <= 58 kHz, 25 kHz < RC/C

; frequency <= 50 kHz, C mode K factor = 2.6.

XOSC0CN\_XFCN\_\_MODE2 EQU 002H ; Select external oscillator mode 2: 58 kHz <

; Crystal frequency <= 155 kHz, 50 kHz < RC/C

; frequency <= 100 kHz, C mode K factor = 7.7.

XOSC0CN\_XFCN\_\_MODE3 EQU 003H ; Select external oscillator mode 3: 155 kHz <

; Crystal frequency <= 415 kHz, 100 kHz < RC/C

; frequency <= 200 kHz, C mode K factor = 22.

XOSC0CN\_XFCN\_\_MODE4 EQU 004H ; Select external oscillator mode 4: 415 kHz <

; Crystal frequency <= 1.1 MHz, 200 kHz < RC/C

; frequency <= 400 kHz, C mode K factor = 65.

XOSC0CN\_XFCN\_\_MODE5 EQU 005H ; Select external oscillator mode 5: 1.1 MHz <

; Crystal frequency <= 3.1 MHz, 400 kHz < RC/C

; frequency <= 800 kHz, C mode K factor = 180.

XOSC0CN\_XFCN\_\_MODE6 EQU 006H ; Select external oscillator mode 6: 3.1 MHz <

; Crystal frequency <= 8.2 kHz, 800 kHz < RC/C

; frequency <= 1.6 MHz, C mode K factor = 664.

XOSC0CN\_XFCN\_\_MODE7 EQU 007H ; Select external oscillator mode 7: 8.2 MHz <

; Crystal frequency <= 25 MHz, 1.6 MHz < RC/C

; frequency <= 3.2 MHz, C mode K factor = 1590.

XOSC0CN\_XOSCMD\_\_FMASK EQU 070H ; External Oscillator Mode

XOSC0CN\_XOSCMD\_\_SHIFT EQU 004H ; External Oscillator Mode

XOSC0CN\_XOSCMD\_\_DISABLED EQU 000H ; External Oscillator circuit disabled.

XOSC0CN\_XOSCMD\_\_CMOS EQU 020H ; External CMOS Clock Mode.

XOSC0CN\_XOSCMD\_\_CMOS\_DIV\_2 EQU 030H ; External CMOS Clock Mode with divide by 2 stage.

XOSC0CN\_XOSCMD\_\_RC\_DIV\_2 EQU 040H ; RC Oscillator Mode with divide by 2 stage.

XOSC0CN\_XOSCMD\_\_C\_DIV\_2 EQU 050H ; Capacitor Oscillator Mode with divide by 2 stage.

XOSC0CN\_XOSCMD\_\_CRYSTAL EQU 060H ; Crystal Oscillator Mode.

XOSC0CN\_XOSCMD\_\_CRYSTAL\_DIV\_2 EQU 070H ; Crystal Oscillator Mode with divide by 2 stage.

XOSC0CN\_XCLKVLD\_\_BMASK EQU 080H ; External Oscillator Valid Flag

XOSC0CN\_XCLKVLD\_\_SHIFT EQU 007H ; External Oscillator Valid Flag

XOSC0CN\_XCLKVLD\_\_NOT\_SET EQU 000H ; External Oscillator is unused or not yet stable.

XOSC0CN\_XCLKVLD\_\_SET EQU 080H ; External Oscillator is running and stable.

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; FLKEY Enums (Flash Lock and Key @ 0xB7)

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FLKEY\_FLKEY\_\_FMASK EQU 0FFH ; Flash Lock and Key

FLKEY\_FLKEY\_\_SHIFT EQU 000H ; Flash Lock and Key

FLKEY\_FLKEY\_\_LOCKED EQU 000H ; Flash is write/erase locked.

FLKEY\_FLKEY\_\_FIRST EQU 001H ; The first key code has been written (0xA5).

FLKEY\_FLKEY\_\_UNLOCKED EQU 002H ; Flash is unlocked (writes/erases allowed).

FLKEY\_FLKEY\_\_DISABLED EQU 003H ; Flash writes/erases are disabled until the next

; reset.

FLKEY\_FLKEY\_\_KEY1 EQU 0A5H ; Flash writes and erases are enabled by writing

; 0xA5 followed by 0xF1 to the FLKEY register.

FLKEY\_FLKEY\_\_KEY2 EQU 0F1H ; Flash writes and erases are enabled by writing

; 0xA5 followed by 0xF1 to the FLKEY register.

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; FLSCL Enums (Flash Scale @ 0xB6)

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FLSCL\_FLRT\_\_BMASK EQU 010H ; Flash Read Timing

FLSCL\_FLRT\_\_SHIFT EQU 004H ; Flash Read Timing

FLSCL\_FLRT\_\_SYSCLK\_BELOW\_25\_MHZ EQU 000H ; SYSCLK <= 25 MHz.

FLSCL\_FLRT\_\_SYSCLK\_BELOW\_48\_MHZ EQU 010H ; SYSCLK <= 48 MHz.

FLSCL\_FOSE\_\_BMASK EQU 080H ; Flash One-Shot Enable

FLSCL\_FOSE\_\_SHIFT EQU 007H ; Flash One-Shot Enable

FLSCL\_FOSE\_\_DISABLED EQU 000H ; Disable the flash one-shot.

FLSCL\_FOSE\_\_ENABLED EQU 080H ; Enable the flash one-shot (recommended).

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; PSCTL Enums (Program Store Control @ 0x8F)

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PSCTL\_PSWE\_\_BMASK EQU 001H ; Program Store Write Enable

PSCTL\_PSWE\_\_SHIFT EQU 000H ; Program Store Write Enable

PSCTL\_PSWE\_\_WRITE\_DISABLED EQU 000H ; Writes to flash program memory disabled.

PSCTL\_PSWE\_\_WRITE\_ENABLED EQU 001H ; Writes to flash program memory enabled; the MOVX

; write instruction targets flash memory.

PSCTL\_PSEE\_\_BMASK EQU 002H ; Program Store Erase Enable

PSCTL\_PSEE\_\_SHIFT EQU 001H ; Program Store Erase Enable

PSCTL\_PSEE\_\_ERASE\_DISABLED EQU 000H ; Flash program memory erasure disabled.

PSCTL\_PSEE\_\_ERASE\_ENABLED EQU 002H ; Flash program memory erasure enabled.

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; HFO0CAL Enums (High Frequency Oscillator Calibration @ 0xB3)

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HFO0CAL\_OSCICL\_\_FMASK EQU 07FH ; Internal Oscillator Calibration

HFO0CAL\_OSCICL\_\_SHIFT EQU 000H ; Internal Oscillator Calibration

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; HFO0CN Enums (High Frequency Oscillator Control @ 0xB2)

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HFO0CN\_IFCN\_\_FMASK EQU 003H ; Oscillator Frequency Divider Control

HFO0CN\_IFCN\_\_SHIFT EQU 000H ; Oscillator Frequency Divider Control

HFO0CN\_IFCN\_\_SYSCLK\_DIV\_8 EQU 000H ; SYSCLK can be derived from Internal H-F Oscillator

; divided by 8 (1.5 MHz).

HFO0CN\_IFCN\_\_SYSCLK\_DIV\_4 EQU 001H ; SYSCLK can be derived from Internal H-F Oscillator

; divided by 4 (3 MHz).

HFO0CN\_IFCN\_\_SYSCLK\_DIV\_2 EQU 002H ; SYSCLK can be derived from Internal H-F Oscillator

; divided by 2 (6 MHz).

HFO0CN\_IFCN\_\_SYSCLK\_DIV\_1 EQU 003H ; SYSCLK can be derived from Internal H-F Oscillator

; divided by 1 (12 MHz).

HFO0CN\_SUSPEND\_\_BMASK EQU 020H ; Oscillator Suspend Enable

HFO0CN\_SUSPEND\_\_SHIFT EQU 005H ; Oscillator Suspend Enable

HFO0CN\_SUSPEND\_\_DISABLED EQU 000H ; The internal oscillator is not in suspend mode.

HFO0CN\_SUSPEND\_\_ENABLED EQU 020H ; Place the internal oscillator in suspend mode.

HFO0CN\_IFRDY\_\_BMASK EQU 040H ; Oscillator Frequency Ready Flag

HFO0CN\_IFRDY\_\_SHIFT EQU 006H ; Oscillator Frequency Ready Flag

HFO0CN\_IFRDY\_\_NOT\_SET EQU 000H ; The Internal High Frequency Oscillator is not

; running at the programmed frequency.

HFO0CN\_IFRDY\_\_SET EQU 040H ; The Internal High Frequency Oscillator is running

; at the programmed frequency.

HFO0CN\_IOSCEN\_\_BMASK EQU 080H ; Oscillator Enable

HFO0CN\_IOSCEN\_\_SHIFT EQU 007H ; Oscillator Enable

HFO0CN\_IOSCEN\_\_DISABLED EQU 000H ; Disable the High Frequency Oscillator.

HFO0CN\_IOSCEN\_\_ENABLED EQU 080H ; Enable the High Frequency Oscillator.

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; EIE1 Enums (Extended Interrupt Enable 1 @ 0xE6)

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EIE1\_ESMB0\_\_BMASK EQU 001H ; SMBus (SMB0) Interrupt Enable

EIE1\_ESMB0\_\_SHIFT EQU 000H ; SMBus (SMB0) Interrupt Enable

EIE1\_ESMB0\_\_DISABLED EQU 000H ; Disable all SMB0 interrupts.

EIE1\_ESMB0\_\_ENABLED EQU 001H ; Enable interrupt requests generated by SMB0.

EIE1\_EUSB0\_\_BMASK EQU 002H ; USB (USB0) Interrupt Enable

EIE1\_EUSB0\_\_SHIFT EQU 001H ; USB (USB0) Interrupt Enable

EIE1\_EUSB0\_\_DISABLED EQU 000H ; Disable all USB0 interrupts.

EIE1\_EUSB0\_\_ENABLED EQU 002H ; Enable interrupt requests generated by USB0.

EIE1\_EWADC0\_\_BMASK EQU 004H ; ADC0 Window Comparison Interrupt Enable

EIE1\_EWADC0\_\_SHIFT EQU 002H ; ADC0 Window Comparison Interrupt Enable

EIE1\_EWADC0\_\_DISABLED EQU 000H ; Disable ADC0 Window Comparison interrupt.

EIE1\_EWADC0\_\_ENABLED EQU 004H ; Enable interrupt requests generated by ADC0 Window

; Compare flag (ADWINT).

EIE1\_EADC0\_\_BMASK EQU 008H ; ADC0 Conversion Complete Interrupt Enable

EIE1\_EADC0\_\_SHIFT EQU 003H ; ADC0 Conversion Complete Interrupt Enable

EIE1\_EADC0\_\_DISABLED EQU 000H ; Disable ADC0 Conversion Complete interrupt.

EIE1\_EADC0\_\_ENABLED EQU 008H ; Enable interrupt requests generated by the ADINT

; flag.

EIE1\_EPCA0\_\_BMASK EQU 010H ; Programmable Counter Array (PCA0) Interrupt Enable

EIE1\_EPCA0\_\_SHIFT EQU 004H ; Programmable Counter Array (PCA0) Interrupt Enable

EIE1\_EPCA0\_\_DISABLED EQU 000H ; Disable all PCA0 interrupts.

EIE1\_EPCA0\_\_ENABLED EQU 010H ; Enable interrupt requests generated by PCA0.

EIE1\_ECP0\_\_BMASK EQU 020H ; Comparator0 (CP0) Interrupt Enable

EIE1\_ECP0\_\_SHIFT EQU 005H ; Comparator0 (CP0) Interrupt Enable

EIE1\_ECP0\_\_DISABLED EQU 000H ; Disable CP0 interrupts.

EIE1\_ECP0\_\_ENABLED EQU 020H ; Enable interrupt requests generated by the

; comparator 0 CPRIF or CPFIF flags.

EIE1\_ECP1\_\_BMASK EQU 040H ; Comparator1 (CP1) Interrupt Enable

EIE1\_ECP1\_\_SHIFT EQU 006H ; Comparator1 (CP1) Interrupt Enable

EIE1\_ECP1\_\_DISABLED EQU 000H ; Disable CP1 interrupts.

EIE1\_ECP1\_\_ENABLED EQU 040H ; Enable interrupt requests generated by the

; comparator 1 CPRIF or CPFIF flags.

EIE1\_ET3\_\_BMASK EQU 080H ; Timer 3 Interrupt Enable

EIE1\_ET3\_\_SHIFT EQU 007H ; Timer 3 Interrupt Enable

EIE1\_ET3\_\_DISABLED EQU 000H ; Disable Timer 3 interrupts.

EIE1\_ET3\_\_ENABLED EQU 080H ; Enable interrupt requests generated by the TF3L or

; TF3H flags.

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; EIE2 Enums (Extended Interrupt Enable 2 @ 0xE7)

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EIE2\_EVBUS\_\_BMASK EQU 001H ; VBUS Level Interrupt Enable

EIE2\_EVBUS\_\_SHIFT EQU 000H ; VBUS Level Interrupt Enable

EIE2\_EVBUS\_\_DISABLED EQU 000H ; Disable all VBUS interrupts.

EIE2\_EVBUS\_\_ENABLED EQU 001H ; Enable interrupt requests generated by VBUS level

; sense.

EIE2\_ES1\_\_BMASK EQU 002H ; UART1 Interrupt Enable

EIE2\_ES1\_\_SHIFT EQU 001H ; UART1 Interrupt Enable

EIE2\_ES1\_\_DISABLED EQU 000H ; Disable UART1 interrupt.

EIE2\_ES1\_\_ENABLED EQU 002H ; Enable UART1 interrupt.

EIE2\_ESMB1\_\_BMASK EQU 008H ; SMBus1 Interrupt Enable

EIE2\_ESMB1\_\_SHIFT EQU 003H ; SMBus1 Interrupt Enable

EIE2\_ESMB1\_\_DISABLED EQU 000H ; Disable all SMB1 interrupts.

EIE2\_ESMB1\_\_ENABLED EQU 008H ; Enable interrupt requests generated by SMB1.

EIE2\_ET4\_\_BMASK EQU 010H ; Timer 4 Interrupt Enable

EIE2\_ET4\_\_SHIFT EQU 004H ; Timer 4 Interrupt Enable

EIE2\_ET4\_\_DISABLED EQU 000H ; Disable Timer 4interrupts.

EIE2\_ET4\_\_ENABLED EQU 010H ; Enable interrupt requests generated by the TF4L or

; TF4H flags.

EIE2\_ET5\_\_BMASK EQU 020H ; Timer 5 Interrupt Enable

EIE2\_ET5\_\_SHIFT EQU 005H ; Timer 5 Interrupt Enable

EIE2\_ET5\_\_DISABLED EQU 000H ; Disable Timer 5 interrupts.

EIE2\_ET5\_\_ENABLED EQU 020H ; Enable interrupt requests generated by the TF5L or

; TF5H flags.

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; EIP1 Enums (Extended Interrupt Priority 1 @ 0xF6)

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EIP1\_PSMB0\_\_BMASK EQU 001H ; SMBus (SMB0) Interrupt Priority Control

EIP1\_PSMB0\_\_SHIFT EQU 000H ; SMBus (SMB0) Interrupt Priority Control

EIP1\_PSMB0\_\_LOW EQU 000H ; SMB0 interrupt set to low priority level.

EIP1\_PSMB0\_\_HIGH EQU 001H ; SMB0 interrupt set to high priority level.

EIP1\_PUSB0\_\_BMASK EQU 002H ; USB (USB0) Interrupt Priority Control

EIP1\_PUSB0\_\_SHIFT EQU 001H ; USB (USB0) Interrupt Priority Control

EIP1\_PUSB0\_\_LOW EQU 000H ; USB0 interrupt set to low priority level.

EIP1\_PUSB0\_\_HIGH EQU 002H ; USB0 interrupt set to high priority level.

EIP1\_PWADC0\_\_BMASK EQU 004H ; ADC0 Window Comparator Interrupt Priority Control

EIP1\_PWADC0\_\_SHIFT EQU 002H ; ADC0 Window Comparator Interrupt Priority Control

EIP1\_PWADC0\_\_LOW EQU 000H ; ADC0 Window interrupt set to low priority level.

EIP1\_PWADC0\_\_HIGH EQU 004H ; ADC0 Window interrupt set to high priority level.

EIP1\_PADC0\_\_BMASK EQU 008H ; ADC0 Conversion Complete Interrupt Priority Control

EIP1\_PADC0\_\_SHIFT EQU 003H ; ADC0 Conversion Complete Interrupt Priority Control

EIP1\_PADC0\_\_LOW EQU 000H ; ADC0 Conversion Complete interrupt set to low

; priority level.

EIP1\_PADC0\_\_HIGH EQU 008H ; ADC0 Conversion Complete interrupt set to high

; priority level.

EIP1\_PPCA0\_\_BMASK EQU 010H ; Programmable Counter Array (PCA0) Interrupt Priority Control

EIP1\_PPCA0\_\_SHIFT EQU 004H ; Programmable Counter Array (PCA0) Interrupt Priority Control

EIP1\_PPCA0\_\_LOW EQU 000H ; PCA0 interrupt set to low priority level.

EIP1\_PPCA0\_\_HIGH EQU 010H ; PCA0 interrupt set to high priority level.

EIP1\_PCP0\_\_BMASK EQU 020H ; Comparator0 (CP0) Interrupt Priority Control

EIP1\_PCP0\_\_SHIFT EQU 005H ; Comparator0 (CP0) Interrupt Priority Control

EIP1\_PCP0\_\_LOW EQU 000H ; CP0 interrupt set to low priority level.

EIP1\_PCP0\_\_HIGH EQU 020H ; CP0 interrupt set to high priority level.

EIP1\_PCP1\_\_BMASK EQU 040H ; Comparator1 (CP1) Interrupt Priority Control

EIP1\_PCP1\_\_SHIFT EQU 006H ; Comparator1 (CP1) Interrupt Priority Control

EIP1\_PCP1\_\_LOW EQU 000H ; CP1 interrupt set to low priority level.

EIP1\_PCP1\_\_HIGH EQU 040H ; CP1 interrupt set to high priority level.

EIP1\_PT3\_\_BMASK EQU 080H ; Timer 3 Interrupt Priority Control

EIP1\_PT3\_\_SHIFT EQU 007H ; Timer 3 Interrupt Priority Control

EIP1\_PT3\_\_LOW EQU 000H ; Timer 3 interrupts set to low priority level.

EIP1\_PT3\_\_HIGH EQU 080H ; Timer 3 interrupts set to high priority level.

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; EIP2 Enums (Extended Interrupt Priority 2 @ 0xF7)

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EIP2\_PVBUS\_\_BMASK EQU 001H ; VBUS Level Interrupt Priority Control

EIP2\_PVBUS\_\_SHIFT EQU 000H ; VBUS Level Interrupt Priority Control

EIP2\_PVBUS\_\_LOW EQU 000H ; VBUS interrupt set to low priority level.

EIP2\_PVBUS\_\_HIGH EQU 001H ; VBUS interrupt set to high priority level.

EIP2\_PS1\_\_BMASK EQU 002H ; UART1 Interrupt Priority Control

EIP2\_PS1\_\_SHIFT EQU 001H ; UART1 Interrupt Priority Control

EIP2\_PS1\_\_LOW EQU 000H ; UART1 interrupt set to low priority level.

EIP2\_PS1\_\_HIGH EQU 002H ; UART1 interrupt set to high priority level.

EIP2\_PSMB1\_\_BMASK EQU 008H ; SMBus1 Interrupt Priority Control

EIP2\_PSMB1\_\_SHIFT EQU 003H ; SMBus1 Interrupt Priority Control

EIP2\_PSMB1\_\_LOW EQU 000H ; SMB1 interrupt set to low priority level.

EIP2\_PSMB1\_\_HIGH EQU 008H ; SMB1 interrupt set to high priority level.

EIP2\_PT4\_\_BMASK EQU 010H ; Timer 4 Interrupt Priority Control

EIP2\_PT4\_\_SHIFT EQU 004H ; Timer 4 Interrupt Priority Control

EIP2\_PT4\_\_LOW EQU 000H ; Timer 4 interrupt set to low priority level.

EIP2\_PT4\_\_HIGH EQU 010H ; Timer 4 interrupt set to high priority level.

EIP2\_PT5\_\_BMASK EQU 020H ; Timer 5 Interrupt Priority Control

EIP2\_PT5\_\_SHIFT EQU 005H ; Timer 5 Interrupt Priority Control

EIP2\_PT5\_\_LOW EQU 000H ; Timer 5 interrupt set to low priority level.

EIP2\_PT5\_\_HIGH EQU 020H ; Timer 5 interrupt set to high priority level.

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; IE Enums (Interrupt Enable @ 0xA8)

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IE\_EX0\_\_BMASK EQU 001H ; External Interrupt 0 Enable

IE\_EX0\_\_SHIFT EQU 000H ; External Interrupt 0 Enable

IE\_EX0\_\_DISABLED EQU 000H ; Disable external interrupt 0.

IE\_EX0\_\_ENABLED EQU 001H ; Enable interrupt requests generated by the INT0

; input.

IE\_ET0\_\_BMASK EQU 002H ; Timer 0 Interrupt Enable

IE\_ET0\_\_SHIFT EQU 001H ; Timer 0 Interrupt Enable

IE\_ET0\_\_DISABLED EQU 000H ; Disable all Timer 0 interrupt.

IE\_ET0\_\_ENABLED EQU 002H ; Enable interrupt requests generated by the TF0

; flag.

IE\_EX1\_\_BMASK EQU 004H ; External Interrupt 1 Enable

IE\_EX1\_\_SHIFT EQU 002H ; External Interrupt 1 Enable

IE\_EX1\_\_DISABLED EQU 000H ; Disable external interrupt 1.

IE\_EX1\_\_ENABLED EQU 004H ; Enable interrupt requests generated by the INT1

; input.

IE\_ET1\_\_BMASK EQU 008H ; Timer 1 Interrupt Enable

IE\_ET1\_\_SHIFT EQU 003H ; Timer 1 Interrupt Enable

IE\_ET1\_\_DISABLED EQU 000H ; Disable all Timer 1 interrupt.

IE\_ET1\_\_ENABLED EQU 008H ; Enable interrupt requests generated by the TF1

; flag.

IE\_ES0\_\_BMASK EQU 010H ; UART0 Interrupt Enable

IE\_ES0\_\_SHIFT EQU 004H ; UART0 Interrupt Enable

IE\_ES0\_\_DISABLED EQU 000H ; Disable UART0 interrupt.

IE\_ES0\_\_ENABLED EQU 010H ; Enable UART0 interrupt.

IE\_ET2\_\_BMASK EQU 020H ; Timer 2 Interrupt Enable

IE\_ET2\_\_SHIFT EQU 005H ; Timer 2 Interrupt Enable

IE\_ET2\_\_DISABLED EQU 000H ; Disable Timer 2 interrupt.

IE\_ET2\_\_ENABLED EQU 020H ; Enable interrupt requests generated by the TF2L or

; TF2H flags.

IE\_ESPI0\_\_BMASK EQU 040H ; SPI0 Interrupt Enable

IE\_ESPI0\_\_SHIFT EQU 006H ; SPI0 Interrupt Enable

IE\_ESPI0\_\_DISABLED EQU 000H ; Disable all SPI0 interrupts.

IE\_ESPI0\_\_ENABLED EQU 040H ; Enable interrupt requests generated by SPI0.

IE\_EA\_\_BMASK EQU 080H ; All Interrupts Enable

IE\_EA\_\_SHIFT EQU 007H ; All Interrupts Enable

IE\_EA\_\_DISABLED EQU 000H ; Disable all interrupt sources.

IE\_EA\_\_ENABLED EQU 080H ; Enable each interrupt according to its individual

; mask setting.

;------------------------------------------------------------------------------

; IP Enums (Interrupt Priority @ 0xB8)

;------------------------------------------------------------------------------

IP\_PX0\_\_BMASK EQU 001H ; External Interrupt 0 Priority Control

IP\_PX0\_\_SHIFT EQU 000H ; External Interrupt 0 Priority Control

IP\_PX0\_\_LOW EQU 000H ; External Interrupt 0 set to low priority level.

IP\_PX0\_\_HIGH EQU 001H ; External Interrupt 0 set to high priority level.

IP\_PT0\_\_BMASK EQU 002H ; Timer 0 Interrupt Priority Control

IP\_PT0\_\_SHIFT EQU 001H ; Timer 0 Interrupt Priority Control

IP\_PT0\_\_LOW EQU 000H ; Timer 0 interrupt set to low priority level.

IP\_PT0\_\_HIGH EQU 002H ; Timer 0 interrupt set to high priority level.

IP\_PX1\_\_BMASK EQU 004H ; External Interrupt 1 Priority Control

IP\_PX1\_\_SHIFT EQU 002H ; External Interrupt 1 Priority Control

IP\_PX1\_\_LOW EQU 000H ; External Interrupt 1 set to low priority level.

IP\_PX1\_\_HIGH EQU 004H ; External Interrupt 1 set to high priority level.

IP\_PT1\_\_BMASK EQU 008H ; Timer 1 Interrupt Priority Control

IP\_PT1\_\_SHIFT EQU 003H ; Timer 1 Interrupt Priority Control

IP\_PT1\_\_LOW EQU 000H ; Timer 1 interrupt set to low priority level.

IP\_PT1\_\_HIGH EQU 008H ; Timer 1 interrupt set to high priority level.

IP\_PS0\_\_BMASK EQU 010H ; UART0 Interrupt Priority Control

IP\_PS0\_\_SHIFT EQU 004H ; UART0 Interrupt Priority Control

IP\_PS0\_\_LOW EQU 000H ; UART0 interrupt set to low priority level.

IP\_PS0\_\_HIGH EQU 010H ; UART0 interrupt set to high priority level.

IP\_PT2\_\_BMASK EQU 020H ; Timer 2 Interrupt Priority Control

IP\_PT2\_\_SHIFT EQU 005H ; Timer 2 Interrupt Priority Control

IP\_PT2\_\_LOW EQU 000H ; Timer 2 interrupt set to low priority level.

IP\_PT2\_\_HIGH EQU 020H ; Timer 2 interrupt set to high priority level.

IP\_PSPI0\_\_BMASK EQU 040H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control

IP\_PSPI0\_\_SHIFT EQU 006H ; Serial Peripheral Interface (SPI0) Interrupt Priority Control

IP\_PSPI0\_\_LOW EQU 000H ; SPI0 interrupt set to low priority level.

IP\_PSPI0\_\_HIGH EQU 040H ; SPI0 interrupt set to high priority level.

;------------------------------------------------------------------------------

; LFO0CN Enums (Low Frequency Oscillator Control @ 0x86)

;------------------------------------------------------------------------------

LFO0CN\_OSCLD\_\_FMASK EQU 003H ; Internal L-F Oscillator Divider Select

LFO0CN\_OSCLD\_\_SHIFT EQU 000H ; Internal L-F Oscillator Divider Select

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_8 EQU 000H ; Divide by 8 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_4 EQU 001H ; Divide by 4 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_2 EQU 002H ; Divide by 2 selected.

LFO0CN\_OSCLD\_\_DIVIDE\_BY\_1 EQU 003H ; Divide by 1 selected.

LFO0CN\_OSCLF\_\_FMASK EQU 03CH ; Internal L-F Oscillator Frequency Control

LFO0CN\_OSCLF\_\_SHIFT EQU 002H ; Internal L-F Oscillator Frequency Control

LFO0CN\_OSCLRDY\_\_BMASK EQU 040H ; Internal L-F Oscillator Ready

LFO0CN\_OSCLRDY\_\_SHIFT EQU 006H ; Internal L-F Oscillator Ready

LFO0CN\_OSCLRDY\_\_NOT\_SET EQU 000H ; Internal L-F Oscillator frequency not stabilized.

LFO0CN\_OSCLRDY\_\_SET EQU 040H ; Internal L-F Oscillator frequency stabilized.

LFO0CN\_OSCLEN\_\_BMASK EQU 080H ; Internal L-F Oscillator Enable

LFO0CN\_OSCLEN\_\_SHIFT EQU 007H ; Internal L-F Oscillator Enable

LFO0CN\_OSCLEN\_\_DISABLED EQU 000H ; Internal L-F Oscillator Disabled.

LFO0CN\_OSCLEN\_\_ENABLED EQU 080H ; Internal L-F Oscillator Enabled.

;------------------------------------------------------------------------------

; XBR0 Enums (Port I/O Crossbar 0 @ 0xE1)

;------------------------------------------------------------------------------

XBR0\_URT0E\_\_BMASK EQU 001H ; UART0 I/O Output Enable

XBR0\_URT0E\_\_SHIFT EQU 000H ; UART0 I/O Output Enable

XBR0\_URT0E\_\_DISABLED EQU 000H ; UART0 I/O unavailable at Port pin.

XBR0\_URT0E\_\_ENABLED EQU 001H ; UART0 TX, RX routed to Port pins P0.4 and P0.5.

XBR0\_SPI0E\_\_BMASK EQU 002H ; SPI I/O Enable

XBR0\_SPI0E\_\_SHIFT EQU 001H ; SPI I/O Enable

XBR0\_SPI0E\_\_DISABLED EQU 000H ; SPI I/O unavailable at Port pins.

XBR0\_SPI0E\_\_ENABLED EQU 002H ; SPI I/O routed to Port pins. The SPI can be

; assigned either 3 or 4 GPIO pins.

XBR0\_SMB0E\_\_BMASK EQU 004H ; SMBus0 I/O Enable

XBR0\_SMB0E\_\_SHIFT EQU 002H ; SMBus0 I/O Enable

XBR0\_SMB0E\_\_DISABLED EQU 000H ; SMBus0 I/O unavailable at Port pins.

XBR0\_SMB0E\_\_ENABLED EQU 004H ; SMBus0 I/O routed to Port pins.

XBR0\_SYSCKE\_\_BMASK EQU 008H ; SYSCLK Output Enable

XBR0\_SYSCKE\_\_SHIFT EQU 003H ; SYSCLK Output Enable

XBR0\_SYSCKE\_\_DISABLED EQU 000H ; SYSCLK unavailable at Port pin.

XBR0\_SYSCKE\_\_ENABLED EQU 008H ; SYSCLK output routed to Port pin.

XBR0\_CP0E\_\_BMASK EQU 010H ; Comparator0 Output Enable

XBR0\_CP0E\_\_SHIFT EQU 004H ; Comparator0 Output Enable

XBR0\_CP0E\_\_DISABLED EQU 000H ; CP0 unavailable at Port pin.

XBR0\_CP0E\_\_ENABLED EQU 010H ; CP0 routed to Port pin.

XBR0\_CP0AE\_\_BMASK EQU 020H ; Comparator0 Asynchronous Output Enable

XBR0\_CP0AE\_\_SHIFT EQU 005H ; Comparator0 Asynchronous Output Enable

XBR0\_CP0AE\_\_DISABLED EQU 000H ; Asynchronous CP0 unavailable at Port pin.

XBR0\_CP0AE\_\_ENABLED EQU 020H ; Asynchronous CP0 routed to Port pin.

XBR0\_CP1E\_\_BMASK EQU 040H ; Comparator1 Output Enable

XBR0\_CP1E\_\_SHIFT EQU 006H ; Comparator1 Output Enable

XBR0\_CP1E\_\_DISABLED EQU 000H ; CP1 unavailable at Port pin.

XBR0\_CP1E\_\_ENABLED EQU 040H ; CP1 routed to Port pin.

XBR0\_CP1AE\_\_BMASK EQU 080H ; Comparator1 Asynchronous Output Enable

XBR0\_CP1AE\_\_SHIFT EQU 007H ; Comparator1 Asynchronous Output Enable

XBR0\_CP1AE\_\_DISABLED EQU 000H ; Asynchronous CP1 unavailable at Port pin.

XBR0\_CP1AE\_\_ENABLED EQU 080H ; Asynchronous CP1 routed to Port pin.

;------------------------------------------------------------------------------

; XBR1 Enums (Port I/O Crossbar 1 @ 0xE2)

;------------------------------------------------------------------------------

XBR1\_PCA0ME\_\_FMASK EQU 007H ; PCA Module I/O Enable

XBR1\_PCA0ME\_\_SHIFT EQU 000H ; PCA Module I/O Enable

XBR1\_PCA0ME\_\_DISABLED EQU 000H ; All PCA I/O unavailable at Port pins.

XBR1\_PCA0ME\_\_CEX0 EQU 001H ; CEX0 routed to Port pin.

XBR1\_PCA0ME\_\_CEX0\_CEX1 EQU 002H ; CEX0, CEX1 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_CEX1\_CEX2 EQU 003H ; CEX0, CEX1, CEX2 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_CEX1\_CEX2\_CEX3 EQU 004H ; CEX0, CEX1, CEX2, CEX3 routed to Port pins.

XBR1\_PCA0ME\_\_CEX0\_CEX1\_CEX2\_CEX3\_CEX4 EQU 005H ; CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins.

XBR1\_ECIE\_\_BMASK EQU 008H ; PCA0 External Counter Input Enable

XBR1\_ECIE\_\_SHIFT EQU 003H ; PCA0 External Counter Input Enable

XBR1\_ECIE\_\_DISABLED EQU 000H ; ECI unavailable at Port pin.

XBR1\_ECIE\_\_ENABLED EQU 008H ; ECI routed to Port pin.

XBR1\_T0E\_\_BMASK EQU 010H ; T0 Enable

XBR1\_T0E\_\_SHIFT EQU 004H ; T0 Enable

XBR1\_T0E\_\_DISABLED EQU 000H ; T0 unavailable at Port pin.

XBR1\_T0E\_\_ENABLED EQU 010H ; T0 routed to Port pin.

XBR1\_T1E\_\_BMASK EQU 020H ; T1 Enable

XBR1\_T1E\_\_SHIFT EQU 005H ; T1 Enable

XBR1\_T1E\_\_DISABLED EQU 000H ; T1 unavailable at Port pin.

XBR1\_T1E\_\_ENABLED EQU 020H ; T1 routed to Port pin.

XBR1\_XBARE\_\_BMASK EQU 040H ; Crossbar Enable

XBR1\_XBARE\_\_SHIFT EQU 006H ; Crossbar Enable

XBR1\_XBARE\_\_DISABLED EQU 000H ; Crossbar disabled.

XBR1\_XBARE\_\_ENABLED EQU 040H ; Crossbar enabled.

XBR1\_WEAKPUD\_\_BMASK EQU 080H ; Port I/O Weak Pullup Disable

XBR1\_WEAKPUD\_\_SHIFT EQU 007H ; Port I/O Weak Pullup Disable

XBR1\_WEAKPUD\_\_PULL\_UPS\_ENABLED EQU 000H ; Weak Pullups enabled (except for Ports whose I/O

; are configured for analog mode).

XBR1\_WEAKPUD\_\_PULL\_UPS\_DISABLED EQU 080H ; Weak Pullups disabled.

;------------------------------------------------------------------------------

; XBR2 Enums (Port I/O Crossbar 2 @ 0xE3)

;------------------------------------------------------------------------------

XBR2\_URT1E\_\_BMASK EQU 001H ; UART1 I/O Output Enable

XBR2\_URT1E\_\_SHIFT EQU 000H ; UART1 I/O Output Enable

XBR2\_URT1E\_\_DISABLED EQU 000H ; UART1 I/O unavailable at Port pin.

XBR2\_URT1E\_\_ENABLED EQU 001H ; UART1 TX, RX routed to Port pins.

XBR2\_SMB1E\_\_BMASK EQU 002H ; SMBus1 I/O Enable

XBR2\_SMB1E\_\_SHIFT EQU 001H ; SMBus1 I/O Enable

XBR2\_SMB1E\_\_DISABLED EQU 000H ; SMBus1 I/O unavailable at Port pins.

XBR2\_SMB1E\_\_ENABLED EQU 002H ; SMBus1 I/O routed to Port pins.

;------------------------------------------------------------------------------

; PCA0CPH0 Enums (PCA Channel 0 Capture Module High Byte @ 0xFC)

;------------------------------------------------------------------------------

PCA0CPH0\_PCA0CPH0\_\_FMASK EQU 0FFH ; PCA Channel 0 Capture Module High Byte

PCA0CPH0\_PCA0CPH0\_\_SHIFT EQU 000H ; PCA Channel 0 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL0 Enums (PCA Channel 0 Capture Module Low Byte @ 0xFB)

;------------------------------------------------------------------------------

PCA0CPL0\_PCA0CPL0\_\_FMASK EQU 0FFH ; PCA Channel 0 Capture Module Low Byte

PCA0CPL0\_PCA0CPL0\_\_SHIFT EQU 000H ; PCA Channel 0 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM0 Enums (PCA Channel 0 Capture/Compare Mode @ 0xDA)

;------------------------------------------------------------------------------

PCA0CPM0\_ECCF\_\_BMASK EQU 001H ; Channel 0 Capture/Compare Flag Interrupt Enable

PCA0CPM0\_ECCF\_\_SHIFT EQU 000H ; Channel 0 Capture/Compare Flag Interrupt Enable

PCA0CPM0\_ECCF\_\_DISABLED EQU 000H ; Disable CCF0 interrupts.

PCA0CPM0\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF0 is set.

PCA0CPM0\_PWM\_\_BMASK EQU 002H ; Channel 0 Pulse Width Modulation Mode Enable

PCA0CPM0\_PWM\_\_SHIFT EQU 001H ; Channel 0 Pulse Width Modulation Mode Enable

PCA0CPM0\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM0\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM0\_TOG\_\_BMASK EQU 004H ; Channel 0 Toggle Function Enable

PCA0CPM0\_TOG\_\_SHIFT EQU 002H ; Channel 0 Toggle Function Enable

PCA0CPM0\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM0\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM0\_MAT\_\_BMASK EQU 008H ; Channel 0 Match Function Enable

PCA0CPM0\_MAT\_\_SHIFT EQU 003H ; Channel 0 Match Function Enable

PCA0CPM0\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM0\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM0\_CAPN\_\_BMASK EQU 010H ; Channel 0 Capture Negative Function Enable

PCA0CPM0\_CAPN\_\_SHIFT EQU 004H ; Channel 0 Capture Negative Function Enable

PCA0CPM0\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM0\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM0\_CAPP\_\_BMASK EQU 020H ; Channel 0 Capture Positive Function Enable

PCA0CPM0\_CAPP\_\_SHIFT EQU 005H ; Channel 0 Capture Positive Function Enable

PCA0CPM0\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM0\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM0\_ECOM\_\_BMASK EQU 040H ; Channel 0 Comparator Function Enable

PCA0CPM0\_ECOM\_\_SHIFT EQU 006H ; Channel 0 Comparator Function Enable

PCA0CPM0\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM0\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM0\_PWM16\_\_BMASK EQU 080H ; Channel 0 16-bit Pulse Width Modulation Enable

PCA0CPM0\_PWM16\_\_SHIFT EQU 007H ; Channel 0 16-bit Pulse Width Modulation Enable

PCA0CPM0\_PWM16\_\_8\_BIT EQU 000H ; 8-bit PWM selected.

PCA0CPM0\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH1 Enums (PCA Channel 1 Capture Module High Byte @ 0xEA)

;------------------------------------------------------------------------------

PCA0CPH1\_PCA0CPH1\_\_FMASK EQU 0FFH ; PCA Channel 1 Capture Module High Byte

PCA0CPH1\_PCA0CPH1\_\_SHIFT EQU 000H ; PCA Channel 1 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL1 Enums (PCA Channel 1 Capture Module Low Byte @ 0xE9)

;------------------------------------------------------------------------------

PCA0CPL1\_PCA0CPL1\_\_FMASK EQU 0FFH ; PCA Channel 1 Capture Module Low Byte

PCA0CPL1\_PCA0CPL1\_\_SHIFT EQU 000H ; PCA Channel 1 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM1 Enums (PCA Channel 1 Capture/Compare Mode @ 0xDB)

;------------------------------------------------------------------------------

PCA0CPM1\_ECCF\_\_BMASK EQU 001H ; Channel 1 Capture/Compare Flag Interrupt Enable

PCA0CPM1\_ECCF\_\_SHIFT EQU 000H ; Channel 1 Capture/Compare Flag Interrupt Enable

PCA0CPM1\_ECCF\_\_DISABLED EQU 000H ; Disable CCF1 interrupts.

PCA0CPM1\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF1 is set.

PCA0CPM1\_PWM\_\_BMASK EQU 002H ; Channel 1 Pulse Width Modulation Mode Enable

PCA0CPM1\_PWM\_\_SHIFT EQU 001H ; Channel 1 Pulse Width Modulation Mode Enable

PCA0CPM1\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM1\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM1\_TOG\_\_BMASK EQU 004H ; Channel 1 Toggle Function Enable

PCA0CPM1\_TOG\_\_SHIFT EQU 002H ; Channel 1 Toggle Function Enable

PCA0CPM1\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM1\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM1\_MAT\_\_BMASK EQU 008H ; Channel 1 Match Function Enable

PCA0CPM1\_MAT\_\_SHIFT EQU 003H ; Channel 1 Match Function Enable

PCA0CPM1\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM1\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM1\_CAPN\_\_BMASK EQU 010H ; Channel 1 Capture Negative Function Enable

PCA0CPM1\_CAPN\_\_SHIFT EQU 004H ; Channel 1 Capture Negative Function Enable

PCA0CPM1\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM1\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM1\_CAPP\_\_BMASK EQU 020H ; Channel 1 Capture Positive Function Enable

PCA0CPM1\_CAPP\_\_SHIFT EQU 005H ; Channel 1 Capture Positive Function Enable

PCA0CPM1\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM1\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM1\_ECOM\_\_BMASK EQU 040H ; Channel 1 Comparator Function Enable

PCA0CPM1\_ECOM\_\_SHIFT EQU 006H ; Channel 1 Comparator Function Enable

PCA0CPM1\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM1\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM1\_PWM16\_\_BMASK EQU 080H ; Channel 1 16-bit Pulse Width Modulation Enable

PCA0CPM1\_PWM16\_\_SHIFT EQU 007H ; Channel 1 16-bit Pulse Width Modulation Enable

PCA0CPM1\_PWM16\_\_8\_BIT EQU 000H ; 8-bit PWM selected.

PCA0CPM1\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH2 Enums (PCA Channel 2 Capture Module High Byte @ 0xEC)

;------------------------------------------------------------------------------

PCA0CPH2\_PCA0CPH2\_\_FMASK EQU 0FFH ; PCA Channel 2 Capture Module High Byte

PCA0CPH2\_PCA0CPH2\_\_SHIFT EQU 000H ; PCA Channel 2 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL2 Enums (PCA Channel 2 Capture Module Low Byte @ 0xEB)

;------------------------------------------------------------------------------

PCA0CPL2\_PCA0CPL2\_\_FMASK EQU 0FFH ; PCA Channel 2 Capture Module Low Byte

PCA0CPL2\_PCA0CPL2\_\_SHIFT EQU 000H ; PCA Channel 2 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM2 Enums (PCA Channel 2 Capture/Compare Mode @ 0xDC)

;------------------------------------------------------------------------------

PCA0CPM2\_ECCF\_\_BMASK EQU 001H ; Channel 2 Capture/Compare Flag Interrupt Enable

PCA0CPM2\_ECCF\_\_SHIFT EQU 000H ; Channel 2 Capture/Compare Flag Interrupt Enable

PCA0CPM2\_ECCF\_\_DISABLED EQU 000H ; Disable CCF2 interrupts.

PCA0CPM2\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF2 is set.

PCA0CPM2\_PWM\_\_BMASK EQU 002H ; Channel 2 Pulse Width Modulation Mode Enable

PCA0CPM2\_PWM\_\_SHIFT EQU 001H ; Channel 2 Pulse Width Modulation Mode Enable

PCA0CPM2\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM2\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM2\_TOG\_\_BMASK EQU 004H ; Channel 2 Toggle Function Enable

PCA0CPM2\_TOG\_\_SHIFT EQU 002H ; Channel 2 Toggle Function Enable

PCA0CPM2\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM2\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM2\_MAT\_\_BMASK EQU 008H ; Channel 2 Match Function Enable

PCA0CPM2\_MAT\_\_SHIFT EQU 003H ; Channel 2 Match Function Enable

PCA0CPM2\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM2\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM2\_CAPN\_\_BMASK EQU 010H ; Channel 2 Capture Negative Function Enable

PCA0CPM2\_CAPN\_\_SHIFT EQU 004H ; Channel 2 Capture Negative Function Enable

PCA0CPM2\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM2\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM2\_CAPP\_\_BMASK EQU 020H ; Channel 2 Capture Positive Function Enable

PCA0CPM2\_CAPP\_\_SHIFT EQU 005H ; Channel 2 Capture Positive Function Enable

PCA0CPM2\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM2\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM2\_ECOM\_\_BMASK EQU 040H ; Channel 2 Comparator Function Enable

PCA0CPM2\_ECOM\_\_SHIFT EQU 006H ; Channel 2 Comparator Function Enable

PCA0CPM2\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM2\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM2\_PWM16\_\_BMASK EQU 080H ; Channel 2 16-bit Pulse Width Modulation Enable

PCA0CPM2\_PWM16\_\_SHIFT EQU 007H ; Channel 2 16-bit Pulse Width Modulation Enable

PCA0CPM2\_PWM16\_\_8\_BIT EQU 000H ; 8-bit PWM selected.

PCA0CPM2\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH3 Enums (PCA Channel 3 Capture Module High Byte @ 0xEE)

;------------------------------------------------------------------------------

PCA0CPH3\_PCA0CPH3\_\_FMASK EQU 0FFH ; PCA Channel 3 Capture Module High Byte

PCA0CPH3\_PCA0CPH3\_\_SHIFT EQU 000H ; PCA Channel 3 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL3 Enums (PCA Channel 3 Capture Module Low Byte @ 0xED)

;------------------------------------------------------------------------------

PCA0CPL3\_PCA0CPL3\_\_FMASK EQU 0FFH ; PCA Channel 3 Capture Module Low Byte

PCA0CPL3\_PCA0CPL3\_\_SHIFT EQU 000H ; PCA Channel 3 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM3 Enums (PCA Channel 3 Capture/Compare Mode @ 0xDD)

;------------------------------------------------------------------------------

PCA0CPM3\_ECCF\_\_BMASK EQU 001H ; Channel 3 Capture/Compare Flag Interrupt Enable

PCA0CPM3\_ECCF\_\_SHIFT EQU 000H ; Channel 3 Capture/Compare Flag Interrupt Enable

PCA0CPM3\_ECCF\_\_DISABLED EQU 000H ; Disable CCF3 interrupts.

PCA0CPM3\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF3 is set.

PCA0CPM3\_PWM\_\_BMASK EQU 002H ; Channel 3 Pulse Width Modulation Mode Enable

PCA0CPM3\_PWM\_\_SHIFT EQU 001H ; Channel 3 Pulse Width Modulation Mode Enable

PCA0CPM3\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM3\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM3\_TOG\_\_BMASK EQU 004H ; Channel 3 Toggle Function Enable

PCA0CPM3\_TOG\_\_SHIFT EQU 002H ; Channel 3 Toggle Function Enable

PCA0CPM3\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM3\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM3\_MAT\_\_BMASK EQU 008H ; Channel 3 Match Function Enable

PCA0CPM3\_MAT\_\_SHIFT EQU 003H ; Channel 3 Match Function Enable

PCA0CPM3\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM3\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM3\_CAPN\_\_BMASK EQU 010H ; Channel 3 Capture Negative Function Enable

PCA0CPM3\_CAPN\_\_SHIFT EQU 004H ; Channel 3 Capture Negative Function Enable

PCA0CPM3\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM3\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM3\_CAPP\_\_BMASK EQU 020H ; Channel 3 Capture Positive Function Enable

PCA0CPM3\_CAPP\_\_SHIFT EQU 005H ; Channel 3 Capture Positive Function Enable

PCA0CPM3\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM3\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM3\_ECOM\_\_BMASK EQU 040H ; Channel 3 Comparator Function Enable

PCA0CPM3\_ECOM\_\_SHIFT EQU 006H ; Channel 3 Comparator Function Enable

PCA0CPM3\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM3\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM3\_PWM16\_\_BMASK EQU 080H ; Channel 3 16-bit Pulse Width Modulation Enable

PCA0CPM3\_PWM16\_\_SHIFT EQU 007H ; Channel 3 16-bit Pulse Width Modulation Enable

PCA0CPM3\_PWM16\_\_8\_BIT EQU 000H ; 8-bit PWM selected.

PCA0CPM3\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CPH4 Enums (PCA Channel 4 Capture Module High Byte @ 0xFE)

;------------------------------------------------------------------------------

PCA0CPH4\_PCA0CPH4\_\_FMASK EQU 0FFH ; PCA Channel 4 Capture Module High Byte

PCA0CPH4\_PCA0CPH4\_\_SHIFT EQU 000H ; PCA Channel 4 Capture Module High Byte

;------------------------------------------------------------------------------

; PCA0CPL4 Enums (PCA Channel 4 Capture Module Low Byte @ 0xFD)

;------------------------------------------------------------------------------

PCA0CPL4\_PCA0CPL4\_\_FMASK EQU 0FFH ; PCA Channel 4 Capture Module Low Byte

PCA0CPL4\_PCA0CPL4\_\_SHIFT EQU 000H ; PCA Channel 4 Capture Module Low Byte

;------------------------------------------------------------------------------

; PCA0CPM4 Enums (PCA Channel 4 Capture/Compare Mode @ 0xDE)

;------------------------------------------------------------------------------

PCA0CPM4\_ECCF\_\_BMASK EQU 001H ; Channel 4 Capture/Compare Flag Interrupt Enable

PCA0CPM4\_ECCF\_\_SHIFT EQU 000H ; Channel 4 Capture/Compare Flag Interrupt Enable

PCA0CPM4\_ECCF\_\_DISABLED EQU 000H ; Disable CCF4 interrupts.

PCA0CPM4\_ECCF\_\_ENABLED EQU 001H ; Enable a Capture/Compare Flag interrupt request

; when CCF4 is set.

PCA0CPM4\_PWM\_\_BMASK EQU 002H ; Channel 4 Pulse Width Modulation Mode Enable

PCA0CPM4\_PWM\_\_SHIFT EQU 001H ; Channel 4 Pulse Width Modulation Mode Enable

PCA0CPM4\_PWM\_\_DISABLED EQU 000H ; Disable PWM function.

PCA0CPM4\_PWM\_\_ENABLED EQU 002H ; Enable PWM function.

PCA0CPM4\_TOG\_\_BMASK EQU 004H ; Channel 4 Toggle Function Enable

PCA0CPM4\_TOG\_\_SHIFT EQU 002H ; Channel 4 Toggle Function Enable

PCA0CPM4\_TOG\_\_DISABLED EQU 000H ; Disable toggle function.

PCA0CPM4\_TOG\_\_ENABLED EQU 004H ; Enable toggle function.

PCA0CPM4\_MAT\_\_BMASK EQU 008H ; Channel 4 Match Function Enable

PCA0CPM4\_MAT\_\_SHIFT EQU 003H ; Channel 4 Match Function Enable

PCA0CPM4\_MAT\_\_DISABLED EQU 000H ; Disable match function.

PCA0CPM4\_MAT\_\_ENABLED EQU 008H ; Enable match function.

PCA0CPM4\_CAPN\_\_BMASK EQU 010H ; Channel 4 Capture Negative Function Enable

PCA0CPM4\_CAPN\_\_SHIFT EQU 004H ; Channel 4 Capture Negative Function Enable

PCA0CPM4\_CAPN\_\_DISABLED EQU 000H ; Disable negative edge capture.

PCA0CPM4\_CAPN\_\_ENABLED EQU 010H ; Enable negative edge capture.

PCA0CPM4\_CAPP\_\_BMASK EQU 020H ; Channel 4 Capture Positive Function Enable

PCA0CPM4\_CAPP\_\_SHIFT EQU 005H ; Channel 4 Capture Positive Function Enable

PCA0CPM4\_CAPP\_\_DISABLED EQU 000H ; Disable positive edge capture.

PCA0CPM4\_CAPP\_\_ENABLED EQU 020H ; Enable positive edge capture.

PCA0CPM4\_ECOM\_\_BMASK EQU 040H ; Channel 4 Comparator Function Enable

PCA0CPM4\_ECOM\_\_SHIFT EQU 006H ; Channel 4 Comparator Function Enable

PCA0CPM4\_ECOM\_\_DISABLED EQU 000H ; Disable comparator function.

PCA0CPM4\_ECOM\_\_ENABLED EQU 040H ; Enable comparator function.

PCA0CPM4\_PWM16\_\_BMASK EQU 080H ; Channel 4 16-bit Pulse Width Modulation Enable

PCA0CPM4\_PWM16\_\_SHIFT EQU 007H ; Channel 4 16-bit Pulse Width Modulation Enable

PCA0CPM4\_PWM16\_\_8\_BIT EQU 000H ; 8-bit PWM selected.

PCA0CPM4\_PWM16\_\_16\_BIT EQU 080H ; 16-bit PWM selected.

;------------------------------------------------------------------------------

; PCA0CN0 Enums (PCA Control 0 @ 0xD8)

;------------------------------------------------------------------------------

PCA0CN0\_CCF0\_\_BMASK EQU 001H ; PCA Module 0 Capture/Compare Flag

PCA0CN0\_CCF0\_\_SHIFT EQU 000H ; PCA Module 0 Capture/Compare Flag

PCA0CN0\_CCF0\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 0.

PCA0CN0\_CCF0\_\_SET EQU 001H ; A match or capture occurred on channel 0.

PCA0CN0\_CCF1\_\_BMASK EQU 002H ; PCA Module 1 Capture/Compare Flag

PCA0CN0\_CCF1\_\_SHIFT EQU 001H ; PCA Module 1 Capture/Compare Flag

PCA0CN0\_CCF1\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 1.

PCA0CN0\_CCF1\_\_SET EQU 002H ; A match or capture occurred on channel 1.

PCA0CN0\_CCF2\_\_BMASK EQU 004H ; PCA Module 2 Capture/Compare Flag

PCA0CN0\_CCF2\_\_SHIFT EQU 002H ; PCA Module 2 Capture/Compare Flag

PCA0CN0\_CCF2\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 2.

PCA0CN0\_CCF2\_\_SET EQU 004H ; A match or capture occurred on channel 2.

PCA0CN0\_CCF3\_\_BMASK EQU 008H ; PCA Module 3 Capture/Compare Flag

PCA0CN0\_CCF3\_\_SHIFT EQU 003H ; PCA Module 3 Capture/Compare Flag

PCA0CN0\_CCF3\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 3.

PCA0CN0\_CCF3\_\_SET EQU 008H ; A match or capture occurred on channel 3.

PCA0CN0\_CCF4\_\_BMASK EQU 010H ; PCA Module 4 Capture/Compare Flag

PCA0CN0\_CCF4\_\_SHIFT EQU 004H ; PCA Module 4 Capture/Compare Flag

PCA0CN0\_CCF4\_\_NOT\_SET EQU 000H ; A match or capture did not occur on channel 4.

PCA0CN0\_CCF4\_\_SET EQU 010H ; A match or capture occurred on channel 4.

PCA0CN0\_CR\_\_BMASK EQU 040H ; PCA Counter/Timer Run Control

PCA0CN0\_CR\_\_SHIFT EQU 006H ; PCA Counter/Timer Run Control

PCA0CN0\_CR\_\_STOP EQU 000H ; Stop the PCA Counter/Timer.

PCA0CN0\_CR\_\_RUN EQU 040H ; Start the PCA Counter/Timer running.

PCA0CN0\_CF\_\_BMASK EQU 080H ; PCA Counter/Timer Overflow Flag

PCA0CN0\_CF\_\_SHIFT EQU 007H ; PCA Counter/Timer Overflow Flag

PCA0CN0\_CF\_\_NOT\_SET EQU 000H ; The PCA counter/timer did not overflow.

PCA0CN0\_CF\_\_SET EQU 080H ; The PCA counter/timer overflowed.

;------------------------------------------------------------------------------

; PCA0H Enums (PCA Counter/Timer High Byte @ 0xFA)

;------------------------------------------------------------------------------

PCA0H\_PCA0H\_\_FMASK EQU 0FFH ; PCA Counter/Timer High Byte

PCA0H\_PCA0H\_\_SHIFT EQU 000H ; PCA Counter/Timer High Byte

;------------------------------------------------------------------------------

; PCA0L Enums (PCA Counter/Timer Low Byte @ 0xF9)

;------------------------------------------------------------------------------

PCA0L\_PCA0L\_\_FMASK EQU 0FFH ; PCA Counter/Timer Low Byte

PCA0L\_PCA0L\_\_SHIFT EQU 000H ; PCA Counter/Timer Low Byte

;------------------------------------------------------------------------------

; PCA0MD Enums (PCA Mode @ 0xD9)

;------------------------------------------------------------------------------

PCA0MD\_ECF\_\_BMASK EQU 001H ; PCA Counter/Timer Overflow Interrupt Enable

PCA0MD\_ECF\_\_SHIFT EQU 000H ; PCA Counter/Timer Overflow Interrupt Enable

PCA0MD\_ECF\_\_OVF\_INT\_DISABLED EQU 000H ; Disable the CF interrupt.

PCA0MD\_ECF\_\_OVF\_INT\_ENABLED EQU 001H ; Enable a PCA Counter/Timer Overflow interrupt

; request when CF is set.

PCA0MD\_CPS\_\_FMASK EQU 00EH ; PCA Counter/Timer Pulse Select

PCA0MD\_CPS\_\_SHIFT EQU 001H ; PCA Counter/Timer Pulse Select

PCA0MD\_CPS\_\_SYSCLK\_DIV\_12 EQU 000H ; System clock divided by 12.

PCA0MD\_CPS\_\_SYSCLK\_DIV\_4 EQU 002H ; System clock divided by 4.

PCA0MD\_CPS\_\_T0\_OVERFLOW EQU 004H ; Timer 0 overflow.

PCA0MD\_CPS\_\_ECI EQU 006H ; High-to-low transitions on ECI (max rate = system

; clock divided by 4).

PCA0MD\_CPS\_\_SYSCLK EQU 008H ; System clock.

PCA0MD\_CPS\_\_EXTOSC\_DIV\_8 EQU 00AH ; External clock divided by 8 (synchronized with the

; system clock).

PCA0MD\_WDLCK\_\_BMASK EQU 020H ; Watchdog Timer Lock

PCA0MD\_WDLCK\_\_SHIFT EQU 005H ; Watchdog Timer Lock

PCA0MD\_WDLCK\_\_UNLOCKED EQU 000H ; Watchdog Timer Enable unlocked.

PCA0MD\_WDLCK\_\_LOCKED EQU 020H ; Watchdog Timer Enable locked.

PCA0MD\_WDTE\_\_BMASK EQU 040H ; Watchdog Timer Enable

PCA0MD\_WDTE\_\_SHIFT EQU 006H ; Watchdog Timer Enable

PCA0MD\_WDTE\_\_DISABLED EQU 000H ; Disable Watchdog Timer.

PCA0MD\_WDTE\_\_ENABLED EQU 040H ; Enable PCA Module 4 as the Watchdog Timer.

PCA0MD\_CIDL\_\_BMASK EQU 080H ; PCA Counter/Timer Idle Control

PCA0MD\_CIDL\_\_SHIFT EQU 007H ; PCA Counter/Timer Idle Control

PCA0MD\_CIDL\_\_NORMAL EQU 000H ; PCA continues to function normally while the

; system controller is in Idle Mode.

PCA0MD\_CIDL\_\_SUSPEND EQU 080H ; PCA operation is suspended while the system

; controller is in Idle Mode.

;------------------------------------------------------------------------------

; PCON0 Enums (Power Control @ 0x87)

;------------------------------------------------------------------------------

PCON0\_IDLE\_\_BMASK EQU 001H ; Idle Mode Select

PCON0\_IDLE\_\_SHIFT EQU 000H ; Idle Mode Select

PCON0\_IDLE\_\_NORMAL EQU 000H ; Idle mode not activated.

PCON0\_IDLE\_\_IDLE EQU 001H ; CPU goes into Idle mode (shuts off clock to CPU,

; but clocks to enabled peripherals are still

; active).

PCON0\_STOP\_\_BMASK EQU 002H ; Stop Mode Select

PCON0\_STOP\_\_SHIFT EQU 001H ; Stop Mode Select

PCON0\_STOP\_\_NORMAL EQU 000H ; Stop mode not activated.

PCON0\_STOP\_\_STOP EQU 002H ; CPU goes into Stop mode (internal oscillator

; stopped).

PCON0\_GF0\_\_BMASK EQU 004H ; General Purpose Flag 0

PCON0\_GF0\_\_SHIFT EQU 002H ; General Purpose Flag 0

PCON0\_GF0\_\_NOT\_SET EQU 000H ; The GF0 flag is not set. Clear the GF0 flag.

PCON0\_GF0\_\_SET EQU 004H ; The GF0 flag is set. Set the GF0 flag.

PCON0\_GF1\_\_BMASK EQU 008H ; General Purpose Flag 1

PCON0\_GF1\_\_SHIFT EQU 003H ; General Purpose Flag 1

PCON0\_GF1\_\_NOT\_SET EQU 000H ; The GF1 flag is not set. Clear the GF1 flag.

PCON0\_GF1\_\_SET EQU 008H ; The GF1 flag is set. Set the GF1 flag.

PCON0\_GF2\_\_BMASK EQU 010H ; General Purpose Flag 2

PCON0\_GF2\_\_SHIFT EQU 004H ; General Purpose Flag 2

PCON0\_GF2\_\_NOT\_SET EQU 000H ; The GF2 flag is not set. Clear the GF2 flag.

PCON0\_GF2\_\_SET EQU 010H ; The GF2 flag is set. Set the GF2 flag.

PCON0\_GF3\_\_BMASK EQU 020H ; General Purpose Flag 3

PCON0\_GF3\_\_SHIFT EQU 005H ; General Purpose Flag 3

PCON0\_GF3\_\_NOT\_SET EQU 000H ; The GF3 flag is not set. Clear the GF3 flag.

PCON0\_GF3\_\_SET EQU 020H ; The GF3 flag is set. Set the GF3 flag.

PCON0\_GF4\_\_BMASK EQU 040H ; General Purpose Flag 4

PCON0\_GF4\_\_SHIFT EQU 006H ; General Purpose Flag 4

PCON0\_GF4\_\_NOT\_SET EQU 000H ; The GF4 flag is not set. Clear the GF4 flag.

PCON0\_GF4\_\_SET EQU 040H ; The GF4 flag is set. Set the GF4 flag.

PCON0\_GF5\_\_BMASK EQU 080H ; General Purpose Flag 5

PCON0\_GF5\_\_SHIFT EQU 007H ; General Purpose Flag 5

PCON0\_GF5\_\_NOT\_SET EQU 000H ; The GF5 flag is not set. Clear the GF5 flag.

PCON0\_GF5\_\_SET EQU 080H ; The GF5 flag is set. Set the GF5 flag.

;------------------------------------------------------------------------------

; P0 Enums (Port 0 Pin Latch @ 0x80)

;------------------------------------------------------------------------------

P0\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Latch

P0\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Latch

P0\_B0\_\_LOW EQU 000H ; P0.0 is low. Set P0.0 to drive low.

P0\_B0\_\_HIGH EQU 001H ; P0.0 is high. Set P0.0 to drive or float high.

P0\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Latch

P0\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Latch

P0\_B1\_\_LOW EQU 000H ; P0.1 is low. Set P0.1 to drive low.

P0\_B1\_\_HIGH EQU 002H ; P0.1 is high. Set P0.1 to drive or float high.

P0\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Latch

P0\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Latch

P0\_B2\_\_LOW EQU 000H ; P0.2 is low. Set P0.2 to drive low.

P0\_B2\_\_HIGH EQU 004H ; P0.2 is high. Set P0.2 to drive or float high.

P0\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Latch

P0\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Latch

P0\_B3\_\_LOW EQU 000H ; P0.3 is low. Set P0.3 to drive low.

P0\_B3\_\_HIGH EQU 008H ; P0.3 is high. Set P0.3 to drive or float high.

P0\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Latch

P0\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Latch

P0\_B4\_\_LOW EQU 000H ; P0.4 is low. Set P0.4 to drive low.

P0\_B4\_\_HIGH EQU 010H ; P0.4 is high. Set P0.4 to drive or float high.

P0\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Latch

P0\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Latch

P0\_B5\_\_LOW EQU 000H ; P0.5 is low. Set P0.5 to drive low.

P0\_B5\_\_HIGH EQU 020H ; P0.5 is high. Set P0.5 to drive or float high.

P0\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Latch

P0\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Latch

P0\_B6\_\_LOW EQU 000H ; P0.6 is low. Set P0.6 to drive low.

P0\_B6\_\_HIGH EQU 040H ; P0.6 is high. Set P0.6 to drive or float high.

P0\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Latch

P0\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Latch

P0\_B7\_\_LOW EQU 000H ; P0.7 is low. Set P0.7 to drive low.

P0\_B7\_\_HIGH EQU 080H ; P0.7 is high. Set P0.7 to drive or float high.

;------------------------------------------------------------------------------

; P0MDIN Enums (Port 0 Input Mode @ 0xF1)

;------------------------------------------------------------------------------

P0MDIN\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Input Mode

P0MDIN\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Input Mode

P0MDIN\_B0\_\_ANALOG EQU 000H ; P0.0 pin is configured for analog mode.

P0MDIN\_B0\_\_DIGITAL EQU 001H ; P0.0 pin is configured for digital mode.

P0MDIN\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Input Mode

P0MDIN\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Input Mode

P0MDIN\_B1\_\_ANALOG EQU 000H ; P0.1 pin is configured for analog mode.

P0MDIN\_B1\_\_DIGITAL EQU 002H ; P0.1 pin is configured for digital mode.

P0MDIN\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Input Mode

P0MDIN\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Input Mode

P0MDIN\_B2\_\_ANALOG EQU 000H ; P0.2 pin is configured for analog mode.

P0MDIN\_B2\_\_DIGITAL EQU 004H ; P0.2 pin is configured for digital mode.

P0MDIN\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Input Mode

P0MDIN\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Input Mode

P0MDIN\_B3\_\_ANALOG EQU 000H ; P0.3 pin is configured for analog mode.

P0MDIN\_B3\_\_DIGITAL EQU 008H ; P0.3 pin is configured for digital mode.

P0MDIN\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Input Mode

P0MDIN\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Input Mode

P0MDIN\_B4\_\_ANALOG EQU 000H ; P0.4 pin is configured for analog mode.

P0MDIN\_B4\_\_DIGITAL EQU 010H ; P0.4 pin is configured for digital mode.

P0MDIN\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Input Mode

P0MDIN\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Input Mode

P0MDIN\_B5\_\_ANALOG EQU 000H ; P0.5 pin is configured for analog mode.

P0MDIN\_B5\_\_DIGITAL EQU 020H ; P0.5 pin is configured for digital mode.

P0MDIN\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Input Mode

P0MDIN\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Input Mode

P0MDIN\_B6\_\_ANALOG EQU 000H ; P0.6 pin is configured for analog mode.

P0MDIN\_B6\_\_DIGITAL EQU 040H ; P0.6 pin is configured for digital mode.

P0MDIN\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Input Mode

P0MDIN\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Input Mode

P0MDIN\_B7\_\_ANALOG EQU 000H ; P0.7 pin is configured for analog mode.

P0MDIN\_B7\_\_DIGITAL EQU 080H ; P0.7 pin is configured for digital mode.

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; P0MDOUT Enums (Port 0 Output Mode @ 0xA4)

;------------------------------------------------------------------------------

P0MDOUT\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Output Mode

P0MDOUT\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Output Mode

P0MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P0.0 output is open-drain.

P0MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P0.0 output is push-pull.

P0MDOUT\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Output Mode

P0MDOUT\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Output Mode

P0MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P0.1 output is open-drain.

P0MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P0.1 output is push-pull.

P0MDOUT\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Output Mode

P0MDOUT\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Output Mode

P0MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P0.2 output is open-drain.

P0MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P0.2 output is push-pull.

P0MDOUT\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Output Mode

P0MDOUT\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Output Mode

P0MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P0.3 output is open-drain.

P0MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P0.3 output is push-pull.

P0MDOUT\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Output Mode

P0MDOUT\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Output Mode

P0MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P0.4 output is open-drain.

P0MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P0.4 output is push-pull.

P0MDOUT\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Output Mode

P0MDOUT\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Output Mode

P0MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P0.5 output is open-drain.

P0MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P0.5 output is push-pull.

P0MDOUT\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Output Mode

P0MDOUT\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Output Mode

P0MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P0.6 output is open-drain.

P0MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P0.6 output is push-pull.

P0MDOUT\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Output Mode

P0MDOUT\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Output Mode

P0MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P0.7 output is open-drain.

P0MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P0.7 output is push-pull.

;------------------------------------------------------------------------------

; P0SKIP Enums (Port 0 Skip @ 0xD4)

;------------------------------------------------------------------------------

P0SKIP\_B0\_\_BMASK EQU 001H ; Port 0 Bit 0 Skip

P0SKIP\_B0\_\_SHIFT EQU 000H ; Port 0 Bit 0 Skip

P0SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P0.0 pin is not skipped by the crossbar.

P0SKIP\_B0\_\_SKIPPED EQU 001H ; P0.0 pin is skipped by the crossbar.

P0SKIP\_B1\_\_BMASK EQU 002H ; Port 0 Bit 1 Skip

P0SKIP\_B1\_\_SHIFT EQU 001H ; Port 0 Bit 1 Skip

P0SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P0.1 pin is not skipped by the crossbar.

P0SKIP\_B1\_\_SKIPPED EQU 002H ; P0.1 pin is skipped by the crossbar.

P0SKIP\_B2\_\_BMASK EQU 004H ; Port 0 Bit 2 Skip

P0SKIP\_B2\_\_SHIFT EQU 002H ; Port 0 Bit 2 Skip

P0SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P0.2 pin is not skipped by the crossbar.

P0SKIP\_B2\_\_SKIPPED EQU 004H ; P0.2 pin is skipped by the crossbar.

P0SKIP\_B3\_\_BMASK EQU 008H ; Port 0 Bit 3 Skip

P0SKIP\_B3\_\_SHIFT EQU 003H ; Port 0 Bit 3 Skip

P0SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P0.3 pin is not skipped by the crossbar.

P0SKIP\_B3\_\_SKIPPED EQU 008H ; P0.3 pin is skipped by the crossbar.

P0SKIP\_B4\_\_BMASK EQU 010H ; Port 0 Bit 4 Skip

P0SKIP\_B4\_\_SHIFT EQU 004H ; Port 0 Bit 4 Skip

P0SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P0.4 pin is not skipped by the crossbar.

P0SKIP\_B4\_\_SKIPPED EQU 010H ; P0.4 pin is skipped by the crossbar.

P0SKIP\_B5\_\_BMASK EQU 020H ; Port 0 Bit 5 Skip

P0SKIP\_B5\_\_SHIFT EQU 005H ; Port 0 Bit 5 Skip

P0SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P0.5 pin is not skipped by the crossbar.

P0SKIP\_B5\_\_SKIPPED EQU 020H ; P0.5 pin is skipped by the crossbar.

P0SKIP\_B6\_\_BMASK EQU 040H ; Port 0 Bit 6 Skip

P0SKIP\_B6\_\_SHIFT EQU 006H ; Port 0 Bit 6 Skip

P0SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P0.6 pin is not skipped by the crossbar.

P0SKIP\_B6\_\_SKIPPED EQU 040H ; P0.6 pin is skipped by the crossbar.

P0SKIP\_B7\_\_BMASK EQU 080H ; Port 0 Bit 7 Skip

P0SKIP\_B7\_\_SHIFT EQU 007H ; Port 0 Bit 7 Skip

P0SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P0.7 pin is not skipped by the crossbar.

P0SKIP\_B7\_\_SKIPPED EQU 080H ; P0.7 pin is skipped by the crossbar.

;------------------------------------------------------------------------------

; P1 Enums (Port 1 Pin Latch @ 0x90)

;------------------------------------------------------------------------------

P1\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Latch

P1\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Latch

P1\_B0\_\_LOW EQU 000H ; P1.0 is low. Set P1.0 to drive low.

P1\_B0\_\_HIGH EQU 001H ; P1.0 is high. Set P1.0 to drive or float high.

P1\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Latch

P1\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Latch

P1\_B1\_\_LOW EQU 000H ; P1.1 is low. Set P1.1 to drive low.

P1\_B1\_\_HIGH EQU 002H ; P1.1 is high. Set P1.1 to drive or float high.

P1\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Latch

P1\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Latch

P1\_B2\_\_LOW EQU 000H ; P1.2 is low. Set P1.2 to drive low.

P1\_B2\_\_HIGH EQU 004H ; P1.2 is high. Set P1.2 to drive or float high.

P1\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Latch

P1\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Latch

P1\_B3\_\_LOW EQU 000H ; P1.3 is low. Set P1.3 to drive low.

P1\_B3\_\_HIGH EQU 008H ; P1.3 is high. Set P1.3 to drive or float high.

P1\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Latch

P1\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Latch

P1\_B4\_\_LOW EQU 000H ; P1.4 is low. Set P1.4 to drive low.

P1\_B4\_\_HIGH EQU 010H ; P1.4 is high. Set P1.4 to drive or float high.

P1\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Latch

P1\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Latch

P1\_B5\_\_LOW EQU 000H ; P1.5 is low. Set P1.5 to drive low.

P1\_B5\_\_HIGH EQU 020H ; P1.5 is high. Set P1.5 to drive or float high.

P1\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Latch

P1\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Latch

P1\_B6\_\_LOW EQU 000H ; P1.6 is low. Set P1.6 to drive low.

P1\_B6\_\_HIGH EQU 040H ; P1.6 is high. Set P1.6 to drive or float high.

P1\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Latch

P1\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Latch

P1\_B7\_\_LOW EQU 000H ; P1.7 is low. Set P1.7 to drive low.

P1\_B7\_\_HIGH EQU 080H ; P1.7 is high. Set P1.7 to drive or float high.

;------------------------------------------------------------------------------

; P1MDIN Enums (Port 1 Input Mode @ 0xF2)

;------------------------------------------------------------------------------

P1MDIN\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Input Mode

P1MDIN\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Input Mode

P1MDIN\_B0\_\_ANALOG EQU 000H ; P1.0 pin is configured for analog mode.

P1MDIN\_B0\_\_DIGITAL EQU 001H ; P1.0 pin is configured for digital mode.

P1MDIN\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Input Mode

P1MDIN\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Input Mode

P1MDIN\_B1\_\_ANALOG EQU 000H ; P1.1 pin is configured for analog mode.

P1MDIN\_B1\_\_DIGITAL EQU 002H ; P1.1 pin is configured for digital mode.

P1MDIN\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Input Mode

P1MDIN\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Input Mode

P1MDIN\_B2\_\_ANALOG EQU 000H ; P1.2 pin is configured for analog mode.

P1MDIN\_B2\_\_DIGITAL EQU 004H ; P1.2 pin is configured for digital mode.

P1MDIN\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Input Mode

P1MDIN\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Input Mode

P1MDIN\_B3\_\_ANALOG EQU 000H ; P1.3 pin is configured for analog mode.

P1MDIN\_B3\_\_DIGITAL EQU 008H ; P1.3 pin is configured for digital mode.

P1MDIN\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Input Mode

P1MDIN\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Input Mode

P1MDIN\_B4\_\_ANALOG EQU 000H ; P1.4 pin is configured for analog mode.

P1MDIN\_B4\_\_DIGITAL EQU 010H ; P1.4 pin is configured for digital mode.

P1MDIN\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Input Mode

P1MDIN\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Input Mode

P1MDIN\_B5\_\_ANALOG EQU 000H ; P1.5 pin is configured for analog mode.

P1MDIN\_B5\_\_DIGITAL EQU 020H ; P1.5 pin is configured for digital mode.

P1MDIN\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Input Mode

P1MDIN\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Input Mode

P1MDIN\_B6\_\_ANALOG EQU 000H ; P1.6 pin is configured for analog mode.

P1MDIN\_B6\_\_DIGITAL EQU 040H ; P1.6 pin is configured for digital mode.

P1MDIN\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Input Mode

P1MDIN\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Input Mode

P1MDIN\_B7\_\_ANALOG EQU 000H ; P1.7 pin is configured for analog mode.

P1MDIN\_B7\_\_DIGITAL EQU 080H ; P1.7 pin is configured for digital mode.

;------------------------------------------------------------------------------

; P1MDOUT Enums (Port 1 Output Mode @ 0xA5)

;------------------------------------------------------------------------------

P1MDOUT\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Output Mode

P1MDOUT\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Output Mode

P1MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P1.0 output is open-drain.

P1MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P1.0 output is push-pull.

P1MDOUT\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Output Mode

P1MDOUT\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Output Mode

P1MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P1.1 output is open-drain.

P1MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P1.1 output is push-pull.

P1MDOUT\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Output Mode

P1MDOUT\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Output Mode

P1MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P1.2 output is open-drain.

P1MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P1.2 output is push-pull.

P1MDOUT\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Output Mode

P1MDOUT\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Output Mode

P1MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P1.3 output is open-drain.

P1MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P1.3 output is push-pull.

P1MDOUT\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Output Mode

P1MDOUT\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Output Mode

P1MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P1.4 output is open-drain.

P1MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P1.4 output is push-pull.

P1MDOUT\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Output Mode

P1MDOUT\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Output Mode

P1MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P1.5 output is open-drain.

P1MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P1.5 output is push-pull.

P1MDOUT\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Output Mode

P1MDOUT\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Output Mode

P1MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P1.6 output is open-drain.

P1MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P1.6 output is push-pull.

P1MDOUT\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Output Mode

P1MDOUT\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Output Mode

P1MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P1.7 output is open-drain.

P1MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P1.7 output is push-pull.

;------------------------------------------------------------------------------

; P1SKIP Enums (Port 1 Skip @ 0xD5)

;------------------------------------------------------------------------------

P1SKIP\_B0\_\_BMASK EQU 001H ; Port 1 Bit 0 Skip

P1SKIP\_B0\_\_SHIFT EQU 000H ; Port 1 Bit 0 Skip

P1SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P1.0 pin is not skipped by the crossbar.

P1SKIP\_B0\_\_SKIPPED EQU 001H ; P1.0 pin is skipped by the crossbar.

P1SKIP\_B1\_\_BMASK EQU 002H ; Port 1 Bit 1 Skip

P1SKIP\_B1\_\_SHIFT EQU 001H ; Port 1 Bit 1 Skip

P1SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P1.1 pin is not skipped by the crossbar.

P1SKIP\_B1\_\_SKIPPED EQU 002H ; P1.1 pin is skipped by the crossbar.

P1SKIP\_B2\_\_BMASK EQU 004H ; Port 1 Bit 2 Skip

P1SKIP\_B2\_\_SHIFT EQU 002H ; Port 1 Bit 2 Skip

P1SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P1.2 pin is not skipped by the crossbar.

P1SKIP\_B2\_\_SKIPPED EQU 004H ; P1.2 pin is skipped by the crossbar.

P1SKIP\_B3\_\_BMASK EQU 008H ; Port 1 Bit 3 Skip

P1SKIP\_B3\_\_SHIFT EQU 003H ; Port 1 Bit 3 Skip

P1SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P1.3 pin is not skipped by the crossbar.

P1SKIP\_B3\_\_SKIPPED EQU 008H ; P1.3 pin is skipped by the crossbar.

P1SKIP\_B4\_\_BMASK EQU 010H ; Port 1 Bit 4 Skip

P1SKIP\_B4\_\_SHIFT EQU 004H ; Port 1 Bit 4 Skip

P1SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P1.4 pin is not skipped by the crossbar.

P1SKIP\_B4\_\_SKIPPED EQU 010H ; P1.4 pin is skipped by the crossbar.

P1SKIP\_B5\_\_BMASK EQU 020H ; Port 1 Bit 5 Skip

P1SKIP\_B5\_\_SHIFT EQU 005H ; Port 1 Bit 5 Skip

P1SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P1.5 pin is not skipped by the crossbar.

P1SKIP\_B5\_\_SKIPPED EQU 020H ; P1.5 pin is skipped by the crossbar.

P1SKIP\_B6\_\_BMASK EQU 040H ; Port 1 Bit 6 Skip

P1SKIP\_B6\_\_SHIFT EQU 006H ; Port 1 Bit 6 Skip

P1SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P1.6 pin is not skipped by the crossbar.

P1SKIP\_B6\_\_SKIPPED EQU 040H ; P1.6 pin is skipped by the crossbar.

P1SKIP\_B7\_\_BMASK EQU 080H ; Port 1 Bit 7 Skip

P1SKIP\_B7\_\_SHIFT EQU 007H ; Port 1 Bit 7 Skip

P1SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P1.7 pin is not skipped by the crossbar.

P1SKIP\_B7\_\_SKIPPED EQU 080H ; P1.7 pin is skipped by the crossbar.

;------------------------------------------------------------------------------

; P2 Enums (Port 2 Pin Latch @ 0xA0)

;------------------------------------------------------------------------------

P2\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Latch

P2\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Latch

P2\_B0\_\_LOW EQU 000H ; P2.0 is low. Set P2.0 to drive low.

P2\_B0\_\_HIGH EQU 001H ; P2.0 is high. Set P2.0 to drive or float high.

P2\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Latch

P2\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Latch

P2\_B1\_\_LOW EQU 000H ; P2.1 is low. Set P2.1 to drive low.

P2\_B1\_\_HIGH EQU 002H ; P2.1 is high. Set P2.1 to drive or float high.

P2\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Latch

P2\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Latch

P2\_B2\_\_LOW EQU 000H ; P2.2 is low. Set P2.2 to drive low.

P2\_B2\_\_HIGH EQU 004H ; P2.2 is high. Set P2.2 to drive or float high.

P2\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Latch

P2\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Latch

P2\_B3\_\_LOW EQU 000H ; P2.3 is low. Set P2.3 to drive low.

P2\_B3\_\_HIGH EQU 008H ; P2.3 is high. Set P2.3 to drive or float high.

P2\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Latch

P2\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Latch

P2\_B4\_\_LOW EQU 000H ; P2.4 is low. Set P2.4 to drive low.

P2\_B4\_\_HIGH EQU 010H ; P2.4 is high. Set P2.4 to drive or float high.

P2\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Latch

P2\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Latch

P2\_B5\_\_LOW EQU 000H ; P2.5 is low. Set P2.5 to drive low.

P2\_B5\_\_HIGH EQU 020H ; P2.5 is high. Set P2.5 to drive or float high.

P2\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Latch

P2\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Latch

P2\_B6\_\_LOW EQU 000H ; P2.6 is low. Set P2.6 to drive low.

P2\_B6\_\_HIGH EQU 040H ; P2.6 is high. Set P2.6 to drive or float high.

P2\_B7\_\_BMASK EQU 080H ; Port 2 Bit 7 Latch

P2\_B7\_\_SHIFT EQU 007H ; Port 2 Bit 7 Latch

P2\_B7\_\_LOW EQU 000H ; P2.7 is low. Set P2.7 to drive low.

P2\_B7\_\_HIGH EQU 080H ; P2.7 is high. Set P2.7 to drive or float high.

;------------------------------------------------------------------------------

; P2MDIN Enums (Port 2 Input Mode @ 0xF3)

;------------------------------------------------------------------------------

P2MDIN\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Input Mode

P2MDIN\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Input Mode

P2MDIN\_B0\_\_ANALOG EQU 000H ; P2.0 pin is configured for analog mode.

P2MDIN\_B0\_\_DIGITAL EQU 001H ; P2.0 pin is configured for digital mode.

P2MDIN\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Input Mode

P2MDIN\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Input Mode

P2MDIN\_B1\_\_ANALOG EQU 000H ; P2.1 pin is configured for analog mode.

P2MDIN\_B1\_\_DIGITAL EQU 002H ; P2.1 pin is configured for digital mode.

P2MDIN\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Input Mode

P2MDIN\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Input Mode

P2MDIN\_B2\_\_ANALOG EQU 000H ; P2.2 pin is configured for analog mode.

P2MDIN\_B2\_\_DIGITAL EQU 004H ; P2.2 pin is configured for digital mode.

P2MDIN\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Input Mode

P2MDIN\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Input Mode

P2MDIN\_B3\_\_ANALOG EQU 000H ; P2.3 pin is configured for analog mode.

P2MDIN\_B3\_\_DIGITAL EQU 008H ; P2.3 pin is configured for digital mode.

P2MDIN\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Input Mode

P2MDIN\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Input Mode

P2MDIN\_B4\_\_ANALOG EQU 000H ; P2.4 pin is configured for analog mode.

P2MDIN\_B4\_\_DIGITAL EQU 010H ; P2.4 pin is configured for digital mode.

P2MDIN\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Input Mode

P2MDIN\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Input Mode

P2MDIN\_B5\_\_ANALOG EQU 000H ; P2.5 pin is configured for analog mode.

P2MDIN\_B5\_\_DIGITAL EQU 020H ; P2.5 pin is configured for digital mode.

P2MDIN\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Input Mode

P2MDIN\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Input Mode

P2MDIN\_B6\_\_ANALOG EQU 000H ; P2.6 pin is configured for analog mode.

P2MDIN\_B6\_\_DIGITAL EQU 040H ; P2.6 pin is configured for digital mode.

P2MDIN\_B7\_\_BMASK EQU 080H ; Port 2 Bit 7 Input Mode

P2MDIN\_B7\_\_SHIFT EQU 007H ; Port 2 Bit 7 Input Mode

P2MDIN\_B7\_\_ANALOG EQU 000H ; P2.7 pin is configured for analog mode.

P2MDIN\_B7\_\_DIGITAL EQU 080H ; P2.7 pin is configured for digital mode.

;------------------------------------------------------------------------------

; P2MDOUT Enums (Port 2 Output Mode @ 0xA6)

;------------------------------------------------------------------------------

P2MDOUT\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Output Mode

P2MDOUT\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Output Mode

P2MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P2.0 output is open-drain.

P2MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P2.0 output is push-pull.

P2MDOUT\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Output Mode

P2MDOUT\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Output Mode

P2MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P2.1 output is open-drain.

P2MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P2.1 output is push-pull.

P2MDOUT\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Output Mode

P2MDOUT\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Output Mode

P2MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P2.2 output is open-drain.

P2MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P2.2 output is push-pull.

P2MDOUT\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Output Mode

P2MDOUT\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Output Mode

P2MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P2.3 output is open-drain.

P2MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P2.3 output is push-pull.

P2MDOUT\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Output Mode

P2MDOUT\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Output Mode

P2MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P2.4 output is open-drain.

P2MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P2.4 output is push-pull.

P2MDOUT\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Output Mode

P2MDOUT\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Output Mode

P2MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P2.5 output is open-drain.

P2MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P2.5 output is push-pull.

P2MDOUT\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Output Mode

P2MDOUT\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Output Mode

P2MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P2.6 output is open-drain.

P2MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P2.6 output is push-pull.

P2MDOUT\_B7\_\_BMASK EQU 080H ; Port 2 Bit 7 Output Mode

P2MDOUT\_B7\_\_SHIFT EQU 007H ; Port 2 Bit 7 Output Mode

P2MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P2.7 output is open-drain.

P2MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P2.7 output is push-pull.

;------------------------------------------------------------------------------

; P2SKIP Enums (Port 2 Skip @ 0xD6)

;------------------------------------------------------------------------------

P2SKIP\_B0\_\_BMASK EQU 001H ; Port 2 Bit 0 Skip

P2SKIP\_B0\_\_SHIFT EQU 000H ; Port 2 Bit 0 Skip

P2SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P2.0 pin is not skipped by the crossbar.

P2SKIP\_B0\_\_SKIPPED EQU 001H ; P2.0 pin is skipped by the crossbar.

P2SKIP\_B1\_\_BMASK EQU 002H ; Port 2 Bit 1 Skip

P2SKIP\_B1\_\_SHIFT EQU 001H ; Port 2 Bit 1 Skip

P2SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P2.1 pin is not skipped by the crossbar.

P2SKIP\_B1\_\_SKIPPED EQU 002H ; P2.1 pin is skipped by the crossbar.

P2SKIP\_B2\_\_BMASK EQU 004H ; Port 2 Bit 2 Skip

P2SKIP\_B2\_\_SHIFT EQU 002H ; Port 2 Bit 2 Skip

P2SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P2.2 pin is not skipped by the crossbar.

P2SKIP\_B2\_\_SKIPPED EQU 004H ; P2.2 pin is skipped by the crossbar.

P2SKIP\_B3\_\_BMASK EQU 008H ; Port 2 Bit 3 Skip

P2SKIP\_B3\_\_SHIFT EQU 003H ; Port 2 Bit 3 Skip

P2SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P2.3 pin is not skipped by the crossbar.

P2SKIP\_B3\_\_SKIPPED EQU 008H ; P2.3 pin is skipped by the crossbar.

P2SKIP\_B4\_\_BMASK EQU 010H ; Port 2 Bit 4 Skip

P2SKIP\_B4\_\_SHIFT EQU 004H ; Port 2 Bit 4 Skip

P2SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P2.4 pin is not skipped by the crossbar.

P2SKIP\_B4\_\_SKIPPED EQU 010H ; P2.4 pin is skipped by the crossbar.

P2SKIP\_B5\_\_BMASK EQU 020H ; Port 2 Bit 5 Skip

P2SKIP\_B5\_\_SHIFT EQU 005H ; Port 2 Bit 5 Skip

P2SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P2.5 pin is not skipped by the crossbar.

P2SKIP\_B5\_\_SKIPPED EQU 020H ; P2.5 pin is skipped by the crossbar.

P2SKIP\_B6\_\_BMASK EQU 040H ; Port 2 Bit 6 Skip

P2SKIP\_B6\_\_SHIFT EQU 006H ; Port 2 Bit 6 Skip

P2SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P2.6 pin is not skipped by the crossbar.

P2SKIP\_B6\_\_SKIPPED EQU 040H ; P2.6 pin is skipped by the crossbar.

P2SKIP\_B7\_\_BMASK EQU 080H ; Port 2 Bit 7 Skip

P2SKIP\_B7\_\_SHIFT EQU 007H ; Port 2 Bit 7 Skip

P2SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P2.7 pin is not skipped by the crossbar.

P2SKIP\_B7\_\_SKIPPED EQU 080H ; P2.7 pin is skipped by the crossbar.

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; P3 Enums (Port 3 Pin Latch @ 0xB0)

;------------------------------------------------------------------------------

P3\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Latch

P3\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Latch

P3\_B0\_\_LOW EQU 000H ; P3.0 is low. Set P3.0 to drive low.

P3\_B0\_\_HIGH EQU 001H ; P3.0 is high. Set P3.0 to drive or float high.

P3\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Latch

P3\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Latch

P3\_B1\_\_LOW EQU 000H ; P3.1 is low. Set P3.1 to drive low.

P3\_B1\_\_HIGH EQU 002H ; P3.1 is high. Set P3.1 to drive or float high.

P3\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Latch

P3\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Latch

P3\_B2\_\_LOW EQU 000H ; P3.2 is low. Set P3.2 to drive low.

P3\_B2\_\_HIGH EQU 004H ; P3.2 is high. Set P3.2 to drive or float high.

P3\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Latch

P3\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Latch

P3\_B3\_\_LOW EQU 000H ; P3.3 is low. Set P3.3 to drive low.

P3\_B3\_\_HIGH EQU 008H ; P3.3 is high. Set P3.3 to drive or float high.

P3\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Latch

P3\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Latch

P3\_B4\_\_LOW EQU 000H ; P3.4 is low. Set P3.4 to drive low.

P3\_B4\_\_HIGH EQU 010H ; P3.4 is high. Set P3.4 to drive or float high.

P3\_B5\_\_BMASK EQU 020H ; Port 3 Bit 5 Latch

P3\_B5\_\_SHIFT EQU 005H ; Port 3 Bit 5 Latch

P3\_B5\_\_LOW EQU 000H ; P3.5 is low. Set P3.5 to drive low.

P3\_B5\_\_HIGH EQU 020H ; P3.5 is high. Set P3.5 to drive or float high.

P3\_B6\_\_BMASK EQU 040H ; Port 3 Bit 6 Latch

P3\_B6\_\_SHIFT EQU 006H ; Port 3 Bit 6 Latch

P3\_B6\_\_LOW EQU 000H ; P3.6 is low. Set P3.6 to drive low.

P3\_B6\_\_HIGH EQU 040H ; P3.6 is high. Set P3.6 to drive or float high.

P3\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Latch

P3\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Latch

P3\_B7\_\_LOW EQU 000H ; P3.7 is low. Set P3.7 to drive low.

P3\_B7\_\_HIGH EQU 080H ; P3.7 is high. Set P3.7 to drive or float high.

;------------------------------------------------------------------------------

; P3MDIN Enums (Port 3 Input Mode @ 0xF4)

;------------------------------------------------------------------------------

P3MDIN\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Input Mode

P3MDIN\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Input Mode

P3MDIN\_B0\_\_ANALOG EQU 000H ; P3.0 pin is configured for analog mode.

P3MDIN\_B0\_\_DIGITAL EQU 001H ; P3.0 pin is configured for digital mode.

P3MDIN\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Input Mode

P3MDIN\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Input Mode

P3MDIN\_B1\_\_ANALOG EQU 000H ; P3.1 pin is configured for analog mode.

P3MDIN\_B1\_\_DIGITAL EQU 002H ; P3.1 pin is configured for digital mode.

P3MDIN\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Input Mode

P3MDIN\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Input Mode

P3MDIN\_B2\_\_ANALOG EQU 000H ; P3.2 pin is configured for analog mode.

P3MDIN\_B2\_\_DIGITAL EQU 004H ; P3.2 pin is configured for digital mode.

P3MDIN\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Input Mode

P3MDIN\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Input Mode

P3MDIN\_B3\_\_ANALOG EQU 000H ; P3.3 pin is configured for analog mode.

P3MDIN\_B3\_\_DIGITAL EQU 008H ; P3.3 pin is configured for digital mode.

P3MDIN\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Input Mode

P3MDIN\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Input Mode

P3MDIN\_B4\_\_ANALOG EQU 000H ; P3.4 pin is configured for analog mode.

P3MDIN\_B4\_\_DIGITAL EQU 010H ; P3.4 pin is configured for digital mode.

P3MDIN\_B5\_\_BMASK EQU 020H ; Port 3 Bit 5 Input Mode

P3MDIN\_B5\_\_SHIFT EQU 005H ; Port 3 Bit 5 Input Mode

P3MDIN\_B5\_\_ANALOG EQU 000H ; P3.5 pin is configured for analog mode.

P3MDIN\_B5\_\_DIGITAL EQU 020H ; P3.5 pin is configured for digital mode.

P3MDIN\_B6\_\_BMASK EQU 040H ; Port 3 Bit 6 Input Mode

P3MDIN\_B6\_\_SHIFT EQU 006H ; Port 3 Bit 6 Input Mode

P3MDIN\_B6\_\_ANALOG EQU 000H ; P3.6 pin is configured for analog mode.

P3MDIN\_B6\_\_DIGITAL EQU 040H ; P3.6 pin is configured for digital mode.

P3MDIN\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Input Mode

P3MDIN\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Input Mode

P3MDIN\_B7\_\_ANALOG EQU 000H ; P3.7 pin is configured for analog mode.

P3MDIN\_B7\_\_DIGITAL EQU 080H ; P3.7 pin is configured for digital mode.

;------------------------------------------------------------------------------

; P3MDOUT Enums (Port 3 Output Mode @ 0xA7)

;------------------------------------------------------------------------------

P3MDOUT\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Output Mode

P3MDOUT\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Output Mode

P3MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P3.0 output is open-drain.

P3MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P3.0 output is push-pull.

P3MDOUT\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Output Mode

P3MDOUT\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Output Mode

P3MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P3.1 output is open-drain.

P3MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P3.1 output is push-pull.

P3MDOUT\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Output Mode

P3MDOUT\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Output Mode

P3MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P3.2 output is open-drain.

P3MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P3.2 output is push-pull.

P3MDOUT\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Output Mode

P3MDOUT\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Output Mode

P3MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P3.3 output is open-drain.

P3MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P3.3 output is push-pull.

P3MDOUT\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Output Mode

P3MDOUT\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Output Mode

P3MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P3.4 output is open-drain.

P3MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P3.4 output is push-pull.

P3MDOUT\_B5\_\_BMASK EQU 020H ; Port 3 Bit 5 Output Mode

P3MDOUT\_B5\_\_SHIFT EQU 005H ; Port 3 Bit 5 Output Mode

P3MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P3.5 output is open-drain.

P3MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P3.5 output is push-pull.

P3MDOUT\_B6\_\_BMASK EQU 040H ; Port 3 Bit 6 Output Mode

P3MDOUT\_B6\_\_SHIFT EQU 006H ; Port 3 Bit 6 Output Mode

P3MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P3.6 output is open-drain.

P3MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P3.6 output is push-pull.

P3MDOUT\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Output Mode

P3MDOUT\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Output Mode

P3MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P3.7 output is open-drain.

P3MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P3.7 output is push-pull.

;------------------------------------------------------------------------------

; P3SKIP Enums (Port 3 Skip @ 0xDF)

;------------------------------------------------------------------------------

P3SKIP\_B0\_\_BMASK EQU 001H ; Port 3 Bit 0 Skip

P3SKIP\_B0\_\_SHIFT EQU 000H ; Port 3 Bit 0 Skip

P3SKIP\_B0\_\_NOT\_SKIPPED EQU 000H ; P3.0 pin is not skipped by the crossbar.

P3SKIP\_B0\_\_SKIPPED EQU 001H ; P3.0 pin is skipped by the crossbar.

P3SKIP\_B1\_\_BMASK EQU 002H ; Port 3 Bit 1 Skip

P3SKIP\_B1\_\_SHIFT EQU 001H ; Port 3 Bit 1 Skip

P3SKIP\_B1\_\_NOT\_SKIPPED EQU 000H ; P3.1 pin is not skipped by the crossbar.

P3SKIP\_B1\_\_SKIPPED EQU 002H ; P3.1 pin is skipped by the crossbar.

P3SKIP\_B2\_\_BMASK EQU 004H ; Port 3 Bit 2 Skip

P3SKIP\_B2\_\_SHIFT EQU 002H ; Port 3 Bit 2 Skip

P3SKIP\_B2\_\_NOT\_SKIPPED EQU 000H ; P3.2 pin is not skipped by the crossbar.

P3SKIP\_B2\_\_SKIPPED EQU 004H ; P3.2 pin is skipped by the crossbar.

P3SKIP\_B3\_\_BMASK EQU 008H ; Port 3 Bit 3 Skip

P3SKIP\_B3\_\_SHIFT EQU 003H ; Port 3 Bit 3 Skip

P3SKIP\_B3\_\_NOT\_SKIPPED EQU 000H ; P3.3 pin is not skipped by the crossbar.

P3SKIP\_B3\_\_SKIPPED EQU 008H ; P3.3 pin is skipped by the crossbar.

P3SKIP\_B4\_\_BMASK EQU 010H ; Port 3 Bit 4 Skip

P3SKIP\_B4\_\_SHIFT EQU 004H ; Port 3 Bit 4 Skip

P3SKIP\_B4\_\_NOT\_SKIPPED EQU 000H ; P3.4 pin is not skipped by the crossbar.

P3SKIP\_B4\_\_SKIPPED EQU 010H ; P3.4 pin is skipped by the crossbar.

P3SKIP\_B5\_\_BMASK EQU 020H ; Port 3 Bit 5 Skip

P3SKIP\_B5\_\_SHIFT EQU 005H ; Port 3 Bit 5 Skip

P3SKIP\_B5\_\_NOT\_SKIPPED EQU 000H ; P3.5 pin is not skipped by the crossbar.

P3SKIP\_B5\_\_SKIPPED EQU 020H ; P3.5 pin is skipped by the crossbar.

P3SKIP\_B6\_\_BMASK EQU 040H ; Port 3 Bit 6 Skip

P3SKIP\_B6\_\_SHIFT EQU 006H ; Port 3 Bit 6 Skip

P3SKIP\_B6\_\_NOT\_SKIPPED EQU 000H ; P3.6 pin is not skipped by the crossbar.

P3SKIP\_B6\_\_SKIPPED EQU 040H ; P3.6 pin is skipped by the crossbar.

P3SKIP\_B7\_\_BMASK EQU 080H ; Port 3 Bit 7 Skip

P3SKIP\_B7\_\_SHIFT EQU 007H ; Port 3 Bit 7 Skip

P3SKIP\_B7\_\_NOT\_SKIPPED EQU 000H ; P3.7 pin is not skipped by the crossbar.

P3SKIP\_B7\_\_SKIPPED EQU 080H ; P3.7 pin is skipped by the crossbar.

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; P4 Enums (Port 4 Pin Latch @ 0xC7)

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P4\_B0\_\_BMASK EQU 001H ; Port 4 Bit 0 Latch

P4\_B0\_\_SHIFT EQU 000H ; Port 4 Bit 0 Latch

P4\_B0\_\_LOW EQU 000H ; P4.0 is low. Set P4.0 to drive low.

P4\_B0\_\_HIGH EQU 001H ; P4.0 is high. Set P4.0 to drive or float high.

P4\_B1\_\_BMASK EQU 002H ; Port 4 Bit 1 Latch

P4\_B1\_\_SHIFT EQU 001H ; Port 4 Bit 1 Latch

P4\_B1\_\_LOW EQU 000H ; P4.1 is low. Set P4.1 to drive low.

P4\_B1\_\_HIGH EQU 002H ; P4.1 is high. Set P4.1 to drive or float high.

P4\_B2\_\_BMASK EQU 004H ; Port 4 Bit 2 Latch

P4\_B2\_\_SHIFT EQU 002H ; Port 4 Bit 2 Latch

P4\_B2\_\_LOW EQU 000H ; P4.2 is low. Set P4.2 to drive low.

P4\_B2\_\_HIGH EQU 004H ; P4.2 is high. Set P4.2 to drive or float high.

P4\_B3\_\_BMASK EQU 008H ; Port 4 Bit 3 Latch

P4\_B3\_\_SHIFT EQU 003H ; Port 4 Bit 3 Latch

P4\_B3\_\_LOW EQU 000H ; P4.3 is low. Set P4.3 to drive low.

P4\_B3\_\_HIGH EQU 008H ; P4.3 is high. Set P4.3 to drive or float high.

P4\_B4\_\_BMASK EQU 010H ; Port 4 Bit 4 Latch

P4\_B4\_\_SHIFT EQU 004H ; Port 4 Bit 4 Latch

P4\_B4\_\_LOW EQU 000H ; P4.4 is low. Set P4.4 to drive low.

P4\_B4\_\_HIGH EQU 010H ; P4.4 is high. Set P4.4 to drive or float high.

P4\_B5\_\_BMASK EQU 020H ; Port 4 Bit 5 Latch

P4\_B5\_\_SHIFT EQU 005H ; Port 4 Bit 5 Latch

P4\_B5\_\_LOW EQU 000H ; P4.5 is low. Set P4.5 to drive low.

P4\_B5\_\_HIGH EQU 020H ; P4.5 is high. Set P4.5 to drive or float high.

P4\_B6\_\_BMASK EQU 040H ; Port 4 Bit 6 Latch

P4\_B6\_\_SHIFT EQU 006H ; Port 4 Bit 6 Latch

P4\_B6\_\_LOW EQU 000H ; P4.6 is low. Set P4.6 to drive low.

P4\_B6\_\_HIGH EQU 040H ; P4.6 is high. Set P4.6 to drive or float high.

P4\_B7\_\_BMASK EQU 080H ; Port 4 Bit 7 Latch

P4\_B7\_\_SHIFT EQU 007H ; Port 4 Bit 7 Latch

P4\_B7\_\_LOW EQU 000H ; P4.7 is low. Set P4.7 to drive low.

P4\_B7\_\_HIGH EQU 080H ; P4.7 is high. Set P4.7 to drive or float high.

;------------------------------------------------------------------------------

; P4MDIN Enums (Port 4 Input Mode @ 0xF5)

;------------------------------------------------------------------------------

P4MDIN\_B0\_\_BMASK EQU 001H ; Port 4 Bit 0 Input Mode

P4MDIN\_B0\_\_SHIFT EQU 000H ; Port 4 Bit 0 Input Mode

P4MDIN\_B0\_\_ANALOG EQU 000H ; P4.0 pin is configured for analog mode.

P4MDIN\_B0\_\_DIGITAL EQU 001H ; P4.0 pin is configured for digital mode.

P4MDIN\_B1\_\_BMASK EQU 002H ; Port 4 Bit 1 Input Mode

P4MDIN\_B1\_\_SHIFT EQU 001H ; Port 4 Bit 1 Input Mode

P4MDIN\_B1\_\_ANALOG EQU 000H ; P4.1 pin is configured for analog mode.

P4MDIN\_B1\_\_DIGITAL EQU 002H ; P4.1 pin is configured for digital mode.

P4MDIN\_B2\_\_BMASK EQU 004H ; Port 4 Bit 2 Input Mode

P4MDIN\_B2\_\_SHIFT EQU 002H ; Port 4 Bit 2 Input Mode

P4MDIN\_B2\_\_ANALOG EQU 000H ; P4.2 pin is configured for analog mode.

P4MDIN\_B2\_\_DIGITAL EQU 004H ; P4.2 pin is configured for digital mode.

P4MDIN\_B3\_\_BMASK EQU 008H ; Port 4 Bit 3 Input Mode

P4MDIN\_B3\_\_SHIFT EQU 003H ; Port 4 Bit 3 Input Mode

P4MDIN\_B3\_\_ANALOG EQU 000H ; P4.3 pin is configured for analog mode.

P4MDIN\_B3\_\_DIGITAL EQU 008H ; P4.3 pin is configured for digital mode.

P4MDIN\_B4\_\_BMASK EQU 010H ; Port 4 Bit 4 Input Mode

P4MDIN\_B4\_\_SHIFT EQU 004H ; Port 4 Bit 4 Input Mode

P4MDIN\_B4\_\_ANALOG EQU 000H ; P4.4 pin is configured for analog mode.

P4MDIN\_B4\_\_DIGITAL EQU 010H ; P4.4 pin is configured for digital mode.

P4MDIN\_B5\_\_BMASK EQU 020H ; Port 4 Bit 5 Input Mode

P4MDIN\_B5\_\_SHIFT EQU 005H ; Port 4 Bit 5 Input Mode

P4MDIN\_B5\_\_ANALOG EQU 000H ; P4.5 pin is configured for analog mode.

P4MDIN\_B5\_\_DIGITAL EQU 020H ; P4.5 pin is configured for digital mode.

P4MDIN\_B6\_\_BMASK EQU 040H ; Port 4 Bit 6 Input Mode

P4MDIN\_B6\_\_SHIFT EQU 006H ; Port 4 Bit 6 Input Mode

P4MDIN\_B6\_\_ANALOG EQU 000H ; P4.6 pin is configured for analog mode.

P4MDIN\_B6\_\_DIGITAL EQU 040H ; P4.6 pin is configured for digital mode.

P4MDIN\_B7\_\_BMASK EQU 080H ; Port 4 Bit 7 Input Mode

P4MDIN\_B7\_\_SHIFT EQU 007H ; Port 4 Bit 7 Input Mode

P4MDIN\_B7\_\_ANALOG EQU 000H ; P4.7 pin is configured for analog mode.

P4MDIN\_B7\_\_DIGITAL EQU 080H ; P4.7 pin is configured for digital mode.

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; P4MDOUT Enums (Port 4 Output Mode @ 0xAE)

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P4MDOUT\_B0\_\_BMASK EQU 001H ; Port 4 Bit 0 Output Mode

P4MDOUT\_B0\_\_SHIFT EQU 000H ; Port 4 Bit 0 Output Mode

P4MDOUT\_B0\_\_OPEN\_DRAIN EQU 000H ; P4.0 output is open-drain.

P4MDOUT\_B0\_\_PUSH\_PULL EQU 001H ; P4.0 output is push-pull.

P4MDOUT\_B1\_\_BMASK EQU 002H ; Port 4 Bit 1 Output Mode

P4MDOUT\_B1\_\_SHIFT EQU 001H ; Port 4 Bit 1 Output Mode

P4MDOUT\_B1\_\_OPEN\_DRAIN EQU 000H ; P4.1 output is open-drain.

P4MDOUT\_B1\_\_PUSH\_PULL EQU 002H ; P4.1 output is push-pull.

P4MDOUT\_B2\_\_BMASK EQU 004H ; Port 4 Bit 2 Output Mode

P4MDOUT\_B2\_\_SHIFT EQU 002H ; Port 4 Bit 2 Output Mode

P4MDOUT\_B2\_\_OPEN\_DRAIN EQU 000H ; P4.2 output is open-drain.

P4MDOUT\_B2\_\_PUSH\_PULL EQU 004H ; P4.2 output is push-pull.

P4MDOUT\_B3\_\_BMASK EQU 008H ; Port 4 Bit 3 Output Mode

P4MDOUT\_B3\_\_SHIFT EQU 003H ; Port 4 Bit 3 Output Mode

P4MDOUT\_B3\_\_OPEN\_DRAIN EQU 000H ; P4.3 output is open-drain.

P4MDOUT\_B3\_\_PUSH\_PULL EQU 008H ; P4.3 output is push-pull.

P4MDOUT\_B4\_\_BMASK EQU 010H ; Port 4 Bit 4 Output Mode

P4MDOUT\_B4\_\_SHIFT EQU 004H ; Port 4 Bit 4 Output Mode

P4MDOUT\_B4\_\_OPEN\_DRAIN EQU 000H ; P4.4 output is open-drain.

P4MDOUT\_B4\_\_PUSH\_PULL EQU 010H ; P4.4 output is push-pull.

P4MDOUT\_B5\_\_BMASK EQU 020H ; Port 4 Bit 5 Output Mode

P4MDOUT\_B5\_\_SHIFT EQU 005H ; Port 4 Bit 5 Output Mode

P4MDOUT\_B5\_\_OPEN\_DRAIN EQU 000H ; P4.5 output is open-drain.

P4MDOUT\_B5\_\_PUSH\_PULL EQU 020H ; P4.5 output is push-pull.

P4MDOUT\_B6\_\_BMASK EQU 040H ; Port 4 Bit 6 Output Mode

P4MDOUT\_B6\_\_SHIFT EQU 006H ; Port 4 Bit 6 Output Mode

P4MDOUT\_B6\_\_OPEN\_DRAIN EQU 000H ; P4.6 output is open-drain.

P4MDOUT\_B6\_\_PUSH\_PULL EQU 040H ; P4.6 output is push-pull.

P4MDOUT\_B7\_\_BMASK EQU 080H ; Port 4 Bit 7 Output Mode

P4MDOUT\_B7\_\_SHIFT EQU 007H ; Port 4 Bit 7 Output Mode

P4MDOUT\_B7\_\_OPEN\_DRAIN EQU 000H ; P4.7 output is open-drain.

P4MDOUT\_B7\_\_PUSH\_PULL EQU 080H ; P4.7 output is push-pull.

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; RSTSRC Enums (Reset Source @ 0xEF)

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RSTSRC\_PINRSF\_\_BMASK EQU 001H ; HW Pin Reset Flag

RSTSRC\_PINRSF\_\_SHIFT EQU 000H ; HW Pin Reset Flag

RSTSRC\_PINRSF\_\_NOT\_SET EQU 000H ; The RSTb pin did not cause the last reset.

RSTSRC\_PINRSF\_\_SET EQU 001H ; The RSTb pin caused the last reset.

RSTSRC\_PORSF\_\_BMASK EQU 002H ; Power-On / Supply Monitor Reset Flag, and Supply Monitor Reset Enable

RSTSRC\_PORSF\_\_SHIFT EQU 001H ; Power-On / Supply Monitor Reset Flag, and Supply Monitor Reset Enable

RSTSRC\_PORSF\_\_NOT\_SET EQU 000H ; A power-on or supply monitor reset did not occur.

RSTSRC\_PORSF\_\_SET EQU 002H ; A power-on or supply monitor reset occurred.

RSTSRC\_MCDRSF\_\_BMASK EQU 004H ; Missing Clock Detector Enable and Flag

RSTSRC\_MCDRSF\_\_SHIFT EQU 002H ; Missing Clock Detector Enable and Flag

RSTSRC\_MCDRSF\_\_NOT\_SET EQU 000H ; A missing clock detector reset did not occur.

RSTSRC\_MCDRSF\_\_SET EQU 004H ; A missing clock detector reset occurred.

RSTSRC\_WDTRSF\_\_BMASK EQU 008H ; Watchdog Timer Reset Flag

RSTSRC\_WDTRSF\_\_SHIFT EQU 003H ; Watchdog Timer Reset Flag

RSTSRC\_WDTRSF\_\_NOT\_SET EQU 000H ; A watchdog timer overflow reset did not occur.

RSTSRC\_WDTRSF\_\_SET EQU 008H ; A watchdog timer overflow reset occurred.

RSTSRC\_SWRSF\_\_BMASK EQU 010H ; Software Reset Force and Flag

RSTSRC\_SWRSF\_\_SHIFT EQU 004H ; Software Reset Force and Flag

RSTSRC\_SWRSF\_\_NOT\_SET EQU 000H ; A software reset did not occur.

RSTSRC\_SWRSF\_\_SET EQU 010H ; A software reset occurred.

RSTSRC\_C0RSEF\_\_BMASK EQU 020H ; Comparator0 Reset Enable and Flag

RSTSRC\_C0RSEF\_\_SHIFT EQU 005H ; Comparator0 Reset Enable and Flag

RSTSRC\_C0RSEF\_\_NOT\_SET EQU 000H ; A Comparator 0 reset did not occur.

RSTSRC\_C0RSEF\_\_SET EQU 020H ; A Comparator 0 reset occurred.

RSTSRC\_FERROR\_\_BMASK EQU 040H ; Flash Error Reset Flag

RSTSRC\_FERROR\_\_SHIFT EQU 006H ; Flash Error Reset Flag

RSTSRC\_FERROR\_\_NOT\_SET EQU 000H ; A flash error reset did not occur.

RSTSRC\_FERROR\_\_SET EQU 040H ; A flash error reset occurred.

RSTSRC\_USBRSF\_\_BMASK EQU 080H ; USB Reset Enable and Flag

RSTSRC\_USBRSF\_\_SHIFT EQU 007H ; USB Reset Enable and Flag

RSTSRC\_USBRSF\_\_NOT\_SET EQU 000H ; A USB0 reset did not occur.

RSTSRC\_USBRSF\_\_SET EQU 080H ; A USB0 reset occurred.

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; SFRPAGE Enums (SFR Page @ 0xBF)

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SFRPAGE\_SFRPAGE\_\_FMASK EQU 0FFH ; SFR Page

SFRPAGE\_SFRPAGE\_\_SHIFT EQU 000H ; SFR Page

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; SMB0ADM Enums (SMBus 0 Slave Address Mask @ 0xCE)

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SMB0ADM\_EHACK\_\_BMASK EQU 001H ; Hardware Acknowledge Enable

SMB0ADM\_EHACK\_\_SHIFT EQU 000H ; Hardware Acknowledge Enable

SMB0ADM\_EHACK\_\_ADR\_ACK\_MANUAL EQU 000H ; Firmware must manually acknowledge all incoming

; address and data bytes.

SMB0ADM\_EHACK\_\_ADR\_ACK\_AUTOMATIC EQU 001H ; Automatic slave address recognition and hardware

; acknowledge is enabled.

SMB0ADM\_SLVM\_\_FMASK EQU 0FEH ; SMBus Slave Address Mask

SMB0ADM\_SLVM\_\_SHIFT EQU 001H ; SMBus Slave Address Mask

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; SMB0ADR Enums (SMBus 0 Slave Address @ 0xCF)

;------------------------------------------------------------------------------

SMB0ADR\_GC\_\_BMASK EQU 001H ; General Call Address Enable

SMB0ADR\_GC\_\_SHIFT EQU 000H ; General Call Address Enable

SMB0ADR\_GC\_\_IGNORED EQU 000H ; General Call Address is ignored.

SMB0ADR\_GC\_\_RECOGNIZED EQU 001H ; General Call Address is recognized.

SMB0ADR\_SLV\_\_FMASK EQU 0FEH ; SMBus Hardware Slave Address

SMB0ADR\_SLV\_\_SHIFT EQU 001H ; SMBus Hardware Slave Address

;------------------------------------------------------------------------------

; SMB0CF Enums (SMBus 0 Configuration @ 0xC1)

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SMB0CF\_SMBCS\_\_FMASK EQU 003H ; SMBus Clock Source Selection

SMB0CF\_SMBCS\_\_SHIFT EQU 000H ; SMBus Clock Source Selection

SMB0CF\_SMBCS\_\_TIMER0 EQU 000H ; Timer 0 Overflow.

SMB0CF\_SMBCS\_\_TIMER1 EQU 001H ; Timer 1 Overflow.

SMB0CF\_SMBCS\_\_TIMER2\_HIGH EQU 002H ; Timer 2 High Byte Overflow.

SMB0CF\_SMBCS\_\_TIMER2\_LOW EQU 003H ; Timer 2 Low Byte Overflow.

SMB0CF\_SMBFTE\_\_BMASK EQU 004H ; SMBus Free Timeout Detection Enable

SMB0CF\_SMBFTE\_\_SHIFT EQU 002H ; SMBus Free Timeout Detection Enable

SMB0CF\_SMBFTE\_\_FREE\_TO\_DISABLED EQU 000H ; Disable bus free timeouts.

SMB0CF\_SMBFTE\_\_FREE\_TO\_ENABLED EQU 004H ; Enable bus free timeouts. The bus the bus will be

; considered free if SCL and SDA remain high for

; more than 10 SMBus clock source periods.

SMB0CF\_SMBTOE\_\_BMASK EQU 008H ; SMBus SCL Timeout Detection Enable

SMB0CF\_SMBTOE\_\_SHIFT EQU 003H ; SMBus SCL Timeout Detection Enable

SMB0CF\_SMBTOE\_\_SCL\_TO\_DISABLED EQU 000H ; Disable SCL low timeouts.

SMB0CF\_SMBTOE\_\_SCL\_TO\_ENABLED EQU 008H ; Enable SCL low timeouts.

SMB0CF\_EXTHOLD\_\_BMASK EQU 010H ; SMBus Setup and Hold Time Extension Enable

SMB0CF\_EXTHOLD\_\_SHIFT EQU 004H ; SMBus Setup and Hold Time Extension Enable

SMB0CF\_EXTHOLD\_\_DISABLED EQU 000H ; Disable SDA extended setup and hold times.

SMB0CF\_EXTHOLD\_\_ENABLED EQU 010H ; Enable SDA extended setup and hold times.

SMB0CF\_BUSY\_\_BMASK EQU 020H ; SMBus Busy Indicator

SMB0CF\_BUSY\_\_SHIFT EQU 005H ; SMBus Busy Indicator

SMB0CF\_BUSY\_\_NOT\_SET EQU 000H ; The bus is not busy.

SMB0CF\_BUSY\_\_SET EQU 020H ; The bus is busy and a transfer is currently in

; progress.

SMB0CF\_INH\_\_BMASK EQU 040H ; SMBus Slave Inhibit

SMB0CF\_INH\_\_SHIFT EQU 006H ; SMBus Slave Inhibit

SMB0CF\_INH\_\_SLAVE\_ENABLED EQU 000H ; Slave states are enabled.

SMB0CF\_INH\_\_SLAVE\_DISABLED EQU 040H ; Slave states are inhibited.

SMB0CF\_ENSMB\_\_BMASK EQU 080H ; SMBus Enable

SMB0CF\_ENSMB\_\_SHIFT EQU 007H ; SMBus Enable

SMB0CF\_ENSMB\_\_DISABLED EQU 000H ; Disable the SMBus module.

SMB0CF\_ENSMB\_\_ENABLED EQU 080H ; Enable the SMBus module.

;------------------------------------------------------------------------------

; SMB0CN0 Enums (SMBus 0 Control @ 0xC0)

;------------------------------------------------------------------------------

SMB0CN0\_SI\_\_BMASK EQU 001H ; SMBus Interrupt Flag

SMB0CN0\_SI\_\_SHIFT EQU 000H ; SMBus Interrupt Flag

SMB0CN0\_SI\_\_NOT\_SET EQU 000H ;

SMB0CN0\_SI\_\_SET EQU 001H ;

SMB0CN0\_ACK\_\_BMASK EQU 002H ; SMBus Acknowledge

SMB0CN0\_ACK\_\_SHIFT EQU 001H ; SMBus Acknowledge

SMB0CN0\_ACK\_\_NOT\_SET EQU 000H ; Generate a NACK, or the response was a NACK.

SMB0CN0\_ACK\_\_SET EQU 002H ; Generate an ACK, or the response was an ACK.

SMB0CN0\_ARBLOST\_\_BMASK EQU 004H ; SMBus Arbitration Lost Indicator

SMB0CN0\_ARBLOST\_\_SHIFT EQU 002H ; SMBus Arbitration Lost Indicator

SMB0CN0\_ARBLOST\_\_NOT\_SET EQU 000H ; No arbitration error.

SMB0CN0\_ARBLOST\_\_ERROR EQU 004H ; Arbitration error occurred.

SMB0CN0\_ACKRQ\_\_BMASK EQU 008H ; SMBus Acknowledge Request

SMB0CN0\_ACKRQ\_\_SHIFT EQU 003H ; SMBus Acknowledge Request

SMB0CN0\_ACKRQ\_\_NOT\_SET EQU 000H ; No ACK requested.

SMB0CN0\_ACKRQ\_\_REQUESTED EQU 008H ; ACK requested.

SMB0CN0\_STO\_\_BMASK EQU 010H ; SMBus Stop Flag

SMB0CN0\_STO\_\_SHIFT EQU 004H ; SMBus Stop Flag

SMB0CN0\_STO\_\_NOT\_SET EQU 000H ; A STOP is not pending.

SMB0CN0\_STO\_\_SET EQU 010H ; Generate a STOP or a STOP is currently pending.

SMB0CN0\_STA\_\_BMASK EQU 020H ; SMBus Start Flag

SMB0CN0\_STA\_\_SHIFT EQU 005H ; SMBus Start Flag

SMB0CN0\_STA\_\_NOT\_SET EQU 000H ; A START was not detected.

SMB0CN0\_STA\_\_SET EQU 020H ; Generate a START, repeated START, or a START is

; currently pending.

SMB0CN0\_TXMODE\_\_BMASK EQU 040H ; SMBus Transmit Mode Indicator

SMB0CN0\_TXMODE\_\_SHIFT EQU 006H ; SMBus Transmit Mode Indicator

SMB0CN0\_TXMODE\_\_RECEIVER EQU 000H ; SMBus in Receiver Mode.

SMB0CN0\_TXMODE\_\_TRANSMITTER EQU 040H ; SMBus in Transmitter Mode.

SMB0CN0\_MASTER\_\_BMASK EQU 080H ; SMBus Master/Slave Indicator

SMB0CN0\_MASTER\_\_SHIFT EQU 007H ; SMBus Master/Slave Indicator

SMB0CN0\_MASTER\_\_SLAVE EQU 000H ; SMBus operating in slave mode.

SMB0CN0\_MASTER\_\_MASTER EQU 080H ; SMBus operating in master mode.

;------------------------------------------------------------------------------

; SMB0DAT Enums (SMBus 0 Data @ 0xC2)

;------------------------------------------------------------------------------

SMB0DAT\_SMB0DAT\_\_FMASK EQU 0FFH ; SMBus 0 Data

SMB0DAT\_SMB0DAT\_\_SHIFT EQU 000H ; SMBus 0 Data

;------------------------------------------------------------------------------

; SMB1ADM Enums (SMBus 1 Slave Address Mask @ 0xCE)

;------------------------------------------------------------------------------

SMB1ADM\_EHACK\_\_BMASK EQU 001H ; Hardware Acknowledge Enable

SMB1ADM\_EHACK\_\_SHIFT EQU 000H ; Hardware Acknowledge Enable

SMB1ADM\_EHACK\_\_ADR\_ACK\_MANUAL EQU 000H ; Firmware must manually acknowledge all incoming

; address and data bytes.

SMB1ADM\_EHACK\_\_ADR\_ACK\_AUTOMATIC EQU 001H ; Automatic slave address recognition and hardware

; acknowledge is enabled.

SMB1ADM\_SLVM\_\_FMASK EQU 0FEH ; SMBus Slave Address Mask

SMB1ADM\_SLVM\_\_SHIFT EQU 001H ; SMBus Slave Address Mask

;------------------------------------------------------------------------------

; SMB1ADR Enums (SMBus 1 Slave Address @ 0xCF)

;------------------------------------------------------------------------------

SMB1ADR\_GC\_\_BMASK EQU 001H ; General Call Address Enable

SMB1ADR\_GC\_\_SHIFT EQU 000H ; General Call Address Enable

SMB1ADR\_GC\_\_IGNORED EQU 000H ; General Call Address is ignored.

SMB1ADR\_GC\_\_RECOGNIZED EQU 001H ; General Call Address is recognized.

SMB1ADR\_SLV\_\_FMASK EQU 0FEH ; SMBus Hardware Slave Address

SMB1ADR\_SLV\_\_SHIFT EQU 001H ; SMBus Hardware Slave Address

;------------------------------------------------------------------------------

; SMB1CF Enums (SMBus 1 Configuration @ 0xC1)

;------------------------------------------------------------------------------

SMB1CF\_SMBCS\_\_FMASK EQU 003H ; SMBus Clock Source Selection

SMB1CF\_SMBCS\_\_SHIFT EQU 000H ; SMBus Clock Source Selection

SMB1CF\_SMBCS\_\_TIMER0 EQU 000H ; Timer 0 Overflow.

SMB1CF\_SMBCS\_\_TIMER5 EQU 001H ; Timer 5 Overflow.

SMB1CF\_SMBCS\_\_TIMER2\_HIGH EQU 002H ; Timer 2 High Byte Overflow.

SMB1CF\_SMBCS\_\_TIMER2\_LOW EQU 003H ; Timer 2 Low Byte Overflow.

SMB1CF\_SMBFTE\_\_BMASK EQU 004H ; SMBus Free Timeout Detection Enable

SMB1CF\_SMBFTE\_\_SHIFT EQU 002H ; SMBus Free Timeout Detection Enable

SMB1CF\_SMBFTE\_\_FREE\_TO\_DISABLED EQU 000H ; Disable bus free timeouts.

SMB1CF\_SMBFTE\_\_FREE\_TO\_ENABLED EQU 004H ; Enable bus free timeouts. The bus the bus will be

; considered free if SCL and SDA remain high for

; more than 10 SMBus clock source periods.

SMB1CF\_SMBTOE\_\_BMASK EQU 008H ; SMBus SCL Timeout Detection Enable

SMB1CF\_SMBTOE\_\_SHIFT EQU 003H ; SMBus SCL Timeout Detection Enable

SMB1CF\_SMBTOE\_\_SCL\_TO\_DISABLED EQU 000H ; Disable SCL low timeouts.

SMB1CF\_SMBTOE\_\_SCL\_TO\_ENABLED EQU 008H ; Enable SCL low timeouts.

SMB1CF\_EXTHOLD\_\_BMASK EQU 010H ; SMBus Setup and Hold Time Extension Enable

SMB1CF\_EXTHOLD\_\_SHIFT EQU 004H ; SMBus Setup and Hold Time Extension Enable

SMB1CF\_EXTHOLD\_\_DISABLED EQU 000H ; Disable SDA extended setup and hold times.

SMB1CF\_EXTHOLD\_\_ENABLED EQU 010H ; Enable SDA extended setup and hold times.

SMB1CF\_BUSY\_\_BMASK EQU 020H ; SMBus Busy Indicator

SMB1CF\_BUSY\_\_SHIFT EQU 005H ; SMBus Busy Indicator

SMB1CF\_BUSY\_\_NOT\_SET EQU 000H ; The bus is not busy.

SMB1CF\_BUSY\_\_SET EQU 020H ; The bus is busy and a transfer is currently in

; progress.

SMB1CF\_INH\_\_BMASK EQU 040H ; SMBus Slave Inhibit

SMB1CF\_INH\_\_SHIFT EQU 006H ; SMBus Slave Inhibit

SMB1CF\_INH\_\_SLAVE\_ENABLED EQU 000H ; Slave states are enabled.

SMB1CF\_INH\_\_SLAVE\_DISABLED EQU 040H ; Slave states are inhibited.

SMB1CF\_ENSMB\_\_BMASK EQU 080H ; SMBus Enable

SMB1CF\_ENSMB\_\_SHIFT EQU 007H ; SMBus Enable

SMB1CF\_ENSMB\_\_DISABLED EQU 000H ; Disable the SMBus module.

SMB1CF\_ENSMB\_\_ENABLED EQU 080H ; Enable the SMBus module.

;------------------------------------------------------------------------------

; SMB1CN0 Enums (SMBus 1 Control @ 0xC0)

;------------------------------------------------------------------------------

SMB1CN0\_SI\_\_BMASK EQU 001H ; SMBus Interrupt Flag

SMB1CN0\_SI\_\_SHIFT EQU 000H ; SMBus Interrupt Flag

SMB1CN0\_SI\_\_NOT\_SET EQU 000H ;

SMB1CN0\_SI\_\_SET EQU 001H ;

SMB1CN0\_ACK\_\_BMASK EQU 002H ; SMBus Acknowledge

SMB1CN0\_ACK\_\_SHIFT EQU 001H ; SMBus Acknowledge

SMB1CN0\_ACK\_\_NOT\_SET EQU 000H ; Generate a NACK, or the response was a NACK.

SMB1CN0\_ACK\_\_SET EQU 002H ; Generate an ACK, or the response was an ACK.

SMB1CN0\_ARBLOST\_\_BMASK EQU 004H ; SMBus Arbitration Lost Indicator

SMB1CN0\_ARBLOST\_\_SHIFT EQU 002H ; SMBus Arbitration Lost Indicator

SMB1CN0\_ARBLOST\_\_NOT\_SET EQU 000H ; No arbitration error.

SMB1CN0\_ARBLOST\_\_ERROR EQU 004H ; Arbitration error occurred.

SMB1CN0\_ACKRQ\_\_BMASK EQU 008H ; SMBus Acknowledge Request

SMB1CN0\_ACKRQ\_\_SHIFT EQU 003H ; SMBus Acknowledge Request

SMB1CN0\_ACKRQ\_\_NOT\_SET EQU 000H ; No ACK requested.

SMB1CN0\_ACKRQ\_\_REQUESTED EQU 008H ; ACK requested.

SMB1CN0\_STO\_\_BMASK EQU 010H ; SMBus Stop Flag

SMB1CN0\_STO\_\_SHIFT EQU 004H ; SMBus Stop Flag

SMB1CN0\_STO\_\_NOT\_SET EQU 000H ; A STOP is not pending.

SMB1CN0\_STO\_\_SET EQU 010H ; Generate a STOP or a STOP is currently pending.

SMB1CN0\_STA\_\_BMASK EQU 020H ; SMBus Start Flag

SMB1CN0\_STA\_\_SHIFT EQU 005H ; SMBus Start Flag

SMB1CN0\_STA\_\_NOT\_SET EQU 000H ; A START was not detected.

SMB1CN0\_STA\_\_SET EQU 020H ; Generate a START, repeated START, or a START is

; currently pending.

SMB1CN0\_TXMODE\_\_BMASK EQU 040H ; SMBus Transmit Mode Indicator

SMB1CN0\_TXMODE\_\_SHIFT EQU 006H ; SMBus Transmit Mode Indicator

SMB1CN0\_TXMODE\_\_RECEIVER EQU 000H ; SMBus in Receiver Mode.

SMB1CN0\_TXMODE\_\_TRANSMITTER EQU 040H ; SMBus in Transmitter Mode.

SMB1CN0\_MASTER\_\_BMASK EQU 080H ; SMBus Master/Slave Indicator

SMB1CN0\_MASTER\_\_SHIFT EQU 007H ; SMBus Master/Slave Indicator

SMB1CN0\_MASTER\_\_SLAVE EQU 000H ; SMBus operating in slave mode.

SMB1CN0\_MASTER\_\_MASTER EQU 080H ; SMBus operating in master mode.

;------------------------------------------------------------------------------

; SMB1DAT Enums (SMBus 1 Data @ 0xC2)

;------------------------------------------------------------------------------

SMB1DAT\_SMB1DAT\_\_FMASK EQU 0FFH ; SMBus 1 Data

SMB1DAT\_SMB1DAT\_\_SHIFT EQU 000H ; SMBus 1 Data

;------------------------------------------------------------------------------

; SMBTC Enums (SMBus Timing and Pin Control @ 0xB9)

;------------------------------------------------------------------------------

SMBTC\_SMB0SDD\_\_FMASK EQU 003H ; SMBus 0 Start Detection Window

SMBTC\_SMB0SDD\_\_SHIFT EQU 000H ; SMBus 0 Start Detection Window

SMBTC\_SMB0SDD\_\_NONE EQU 000H ; No additional hold time window (0-1 SYSCLK).

SMBTC\_SMB0SDD\_\_ADD\_2\_SYSCLKS EQU 001H ; Increase hold time window to 2-3 SYSCLKs.

SMBTC\_SMB0SDD\_\_ADD\_4\_SYSCLKS EQU 002H ; Increase hold time window to 4-5 SYSCLKs.

SMBTC\_SMB0SDD\_\_ADD\_8\_SYSCLKS EQU 003H ; Increase hold time window to 8-9 SYSCLKs.

SMBTC\_SMB1SDD\_\_FMASK EQU 00CH ; SMBus 1 Start Detection Window

SMBTC\_SMB1SDD\_\_SHIFT EQU 002H ; SMBus 1 Start Detection Window

SMBTC\_SMB1SDD\_\_NONE EQU 000H ; No additional hold time requirement (0-1 SYSCLK).

SMBTC\_SMB1SDD\_\_ADD\_2\_SYSCLKS EQU 004H ; Increase hold time window to 2-3 SYSCLKs.

SMBTC\_SMB1SDD\_\_ADD\_4\_SYSCLKS EQU 008H ; Increase hold time window to 4-5 SYSCLKs.

SMBTC\_SMB1SDD\_\_ADD\_8\_SYSCLKS EQU 00CH ; Increase hold time window to 8-9 SYSCLKs.

;------------------------------------------------------------------------------

; SPI0CFG Enums (SPI0 Configuration @ 0xA1)

;------------------------------------------------------------------------------

SPI0CFG\_RXBMT\_\_BMASK EQU 001H ; Receive Buffer Empty

SPI0CFG\_RXBMT\_\_SHIFT EQU 000H ; Receive Buffer Empty

SPI0CFG\_RXBMT\_\_NOT\_SET EQU 000H ; New data is available in the receive buffer (Slave

; mode).

SPI0CFG\_RXBMT\_\_SET EQU 001H ; No new data in the receive buffer (Slave mode).

SPI0CFG\_SRMT\_\_BMASK EQU 002H ; Shift Register Empty

SPI0CFG\_SRMT\_\_SHIFT EQU 001H ; Shift Register Empty

SPI0CFG\_SRMT\_\_NOT\_SET EQU 000H ; The shift register is not empty.

SPI0CFG\_SRMT\_\_SET EQU 002H ; The shift register is empty.

SPI0CFG\_NSSIN\_\_BMASK EQU 004H ; NSS Instantaneous Pin Input

SPI0CFG\_NSSIN\_\_SHIFT EQU 002H ; NSS Instantaneous Pin Input

SPI0CFG\_NSSIN\_\_LOW EQU 000H ; The NSS pin is low.

SPI0CFG\_NSSIN\_\_HIGH EQU 004H ; The NSS pin is high.

SPI0CFG\_SLVSEL\_\_BMASK EQU 008H ; Slave Selected Flag

SPI0CFG\_SLVSEL\_\_SHIFT EQU 003H ; Slave Selected Flag

SPI0CFG\_SLVSEL\_\_NOT\_SELECTED EQU 000H ; The Slave is not selected (NSS is high).

SPI0CFG\_SLVSEL\_\_SELECTED EQU 008H ; The Slave is selected (NSS is low).

SPI0CFG\_CKPOL\_\_BMASK EQU 010H ; SPI0 Clock Polarity

SPI0CFG\_CKPOL\_\_SHIFT EQU 004H ; SPI0 Clock Polarity

SPI0CFG\_CKPOL\_\_IDLE\_LOW EQU 000H ; SCK line low in idle state.

SPI0CFG\_CKPOL\_\_IDLE\_HIGH EQU 010H ; SCK line high in idle state.

SPI0CFG\_CKPHA\_\_BMASK EQU 020H ; SPI0 Clock Phase

SPI0CFG\_CKPHA\_\_SHIFT EQU 005H ; SPI0 Clock Phase

SPI0CFG\_CKPHA\_\_DATA\_CENTERED\_FIRST EQU 000H ; Data centered on first edge of SCK period.

SPI0CFG\_CKPHA\_\_DATA\_CENTERED\_SECOND EQU 020H ; Data centered on second edge of SCK period.

SPI0CFG\_MSTEN\_\_BMASK EQU 040H ; Master Mode Enable

SPI0CFG\_MSTEN\_\_SHIFT EQU 006H ; Master Mode Enable

SPI0CFG\_MSTEN\_\_MASTER\_DISABLED EQU 000H ; Disable master mode. Operate in slave mode.

SPI0CFG\_MSTEN\_\_MASTER\_ENABLED EQU 040H ; Enable master mode. Operate as a master.

SPI0CFG\_SPIBSY\_\_BMASK EQU 080H ; SPI Busy

SPI0CFG\_SPIBSY\_\_SHIFT EQU 007H ; SPI Busy

SPI0CFG\_SPIBSY\_\_NOT\_SET EQU 000H ; A SPI transfer is not in progress.

SPI0CFG\_SPIBSY\_\_SET EQU 080H ; A SPI transfer is in progress.

;------------------------------------------------------------------------------

; SPI0CKR Enums (SPI0 Clock Rate @ 0xA2)

;------------------------------------------------------------------------------

SPI0CKR\_SPI0CKR\_\_FMASK EQU 0FFH ; SPI0 Clock Rate

SPI0CKR\_SPI0CKR\_\_SHIFT EQU 000H ; SPI0 Clock Rate

;------------------------------------------------------------------------------

; SPI0CN0 Enums (SPI0 Control @ 0xF8)

;------------------------------------------------------------------------------

SPI0CN0\_SPIEN\_\_BMASK EQU 001H ; SPI0 Enable

SPI0CN0\_SPIEN\_\_SHIFT EQU 000H ; SPI0 Enable

SPI0CN0\_SPIEN\_\_DISABLED EQU 000H ; Disable the SPI module.

SPI0CN0\_SPIEN\_\_ENABLED EQU 001H ; Enable the SPI module.

SPI0CN0\_TXBMT\_\_BMASK EQU 002H ; Transmit Buffer Empty

SPI0CN0\_TXBMT\_\_SHIFT EQU 001H ; Transmit Buffer Empty

SPI0CN0\_TXBMT\_\_NOT\_SET EQU 000H ; The transmit buffer is not empty.

SPI0CN0\_TXBMT\_\_SET EQU 002H ; The transmit buffer is empty.

SPI0CN0\_NSSMD\_\_FMASK EQU 00CH ; Slave Select Mode

SPI0CN0\_NSSMD\_\_SHIFT EQU 002H ; Slave Select Mode

SPI0CN0\_NSSMD\_\_3\_WIRE EQU 000H ; 3-Wire Slave or 3-Wire Master Mode. NSS signal is

; not routed to a port pin.

SPI0CN0\_NSSMD\_\_4\_WIRE\_SLAVE EQU 004H ; 4-Wire Slave or Multi-Master Mode. NSS is an input

; to the device.

SPI0CN0\_NSSMD\_\_4\_WIRE\_MASTER\_NSS\_LOW EQU 008H ; 4-Wire Single-Master Mode. NSS is an output and

; logic low.

SPI0CN0\_NSSMD\_\_4\_WIRE\_MASTER\_NSS\_HIGH EQU 00CH ; 4-Wire Single-Master Mode. NSS is an output and

; logic high.

SPI0CN0\_RXOVRN\_\_BMASK EQU 010H ; Receive Overrun Flag

SPI0CN0\_RXOVRN\_\_SHIFT EQU 004H ; Receive Overrun Flag

SPI0CN0\_RXOVRN\_\_NOT\_SET EQU 000H ; A receive overrun did not occur.

SPI0CN0\_RXOVRN\_\_SET EQU 010H ; A receive overrun occurred.

SPI0CN0\_MODF\_\_BMASK EQU 020H ; Mode Fault Flag

SPI0CN0\_MODF\_\_SHIFT EQU 005H ; Mode Fault Flag

SPI0CN0\_MODF\_\_NOT\_SET EQU 000H ; A master collision did not occur.

SPI0CN0\_MODF\_\_SET EQU 020H ; A master collision occurred.

SPI0CN0\_WCOL\_\_BMASK EQU 040H ; Write Collision Flag

SPI0CN0\_WCOL\_\_SHIFT EQU 006H ; Write Collision Flag

SPI0CN0\_WCOL\_\_NOT\_SET EQU 000H ; A write collision did not occur.

SPI0CN0\_WCOL\_\_SET EQU 040H ; A write collision occurred.

SPI0CN0\_SPIF\_\_BMASK EQU 080H ; SPI0 Interrupt Flag

SPI0CN0\_SPIF\_\_SHIFT EQU 007H ; SPI0 Interrupt Flag

SPI0CN0\_SPIF\_\_NOT\_SET EQU 000H ; A data transfer has not completed since the last

; time SPIF was cleared.

SPI0CN0\_SPIF\_\_SET EQU 080H ; A data transfer completed.

;------------------------------------------------------------------------------

; SPI0DAT Enums (SPI0 Data @ 0xA3)

;------------------------------------------------------------------------------

SPI0DAT\_SPI0DAT\_\_FMASK EQU 0FFH ; SPI0 Transmit and Receive Data

SPI0DAT\_SPI0DAT\_\_SHIFT EQU 000H ; SPI0 Transmit and Receive Data

;------------------------------------------------------------------------------

; TH0 Enums (Timer 0 High Byte @ 0x8C)

;------------------------------------------------------------------------------

TH0\_TH0\_\_FMASK EQU 0FFH ; Timer 0 High Byte

TH0\_TH0\_\_SHIFT EQU 000H ; Timer 0 High Byte

;------------------------------------------------------------------------------

; TH1 Enums (Timer 1 High Byte @ 0x8D)

;------------------------------------------------------------------------------

TH1\_TH1\_\_FMASK EQU 0FFH ; Timer 1 High Byte

TH1\_TH1\_\_SHIFT EQU 000H ; Timer 1 High Byte

;------------------------------------------------------------------------------

; TL0 Enums (Timer 0 Low Byte @ 0x8A)

;------------------------------------------------------------------------------

TL0\_TL0\_\_FMASK EQU 0FFH ; Timer 0 Low Byte

TL0\_TL0\_\_SHIFT EQU 000H ; Timer 0 Low Byte

;------------------------------------------------------------------------------

; TL1 Enums (Timer 1 Low Byte @ 0x8B)

;------------------------------------------------------------------------------

TL1\_TL1\_\_FMASK EQU 0FFH ; Timer 1 Low Byte

TL1\_TL1\_\_SHIFT EQU 000H ; Timer 1 Low Byte

;------------------------------------------------------------------------------

; TMR2CN0 Enums (Timer 2 Control 0 @ 0xC8)

;------------------------------------------------------------------------------

TMR2CN0\_T2XCLK\_\_BMASK EQU 001H ; Timer 2 External Clock Select

TMR2CN0\_T2XCLK\_\_SHIFT EQU 000H ; Timer 2 External Clock Select

TMR2CN0\_T2XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 2 clock is the system clock divided by 12.

TMR2CN0\_T2XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 2 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK).

TMR2CN0\_T2CSS\_\_BMASK EQU 002H ; Timer 2 Capture Source Select

TMR2CN0\_T2CSS\_\_SHIFT EQU 001H ; Timer 2 Capture Source Select

TMR2CN0\_T2CSS\_\_USB\_SOF\_CAPTURE EQU 000H ; Capture source is USB SOF event.

TMR2CN0\_T2CSS\_\_LFOSC\_CAPTURE EQU 002H ; Capture source is falling edge of Low-Frequency

; Oscillator.

TMR2CN0\_TR2\_\_BMASK EQU 004H ; Timer 2 Run Control

TMR2CN0\_TR2\_\_SHIFT EQU 002H ; Timer 2 Run Control

TMR2CN0\_TR2\_\_STOP EQU 000H ; Stop Timer 2.

TMR2CN0\_TR2\_\_RUN EQU 004H ; Start Timer 2 running.

TMR2CN0\_T2SPLIT\_\_BMASK EQU 008H ; Timer 2 Split Mode Enable

TMR2CN0\_T2SPLIT\_\_SHIFT EQU 003H ; Timer 2 Split Mode Enable

TMR2CN0\_T2SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 2 operates in 16-bit auto-reload mode.

TMR2CN0\_T2SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 2 operates as two 8-bit auto-reload timers.

TMR2CN0\_TF2CEN\_\_BMASK EQU 010H ; Timer 2 Capture Enable

TMR2CN0\_TF2CEN\_\_SHIFT EQU 004H ; Timer 2 Capture Enable

TMR2CN0\_TF2CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR2CN0\_TF2CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR2CN0\_TF2LEN\_\_BMASK EQU 020H ; Timer 2 Low Byte Interrupt Enable

TMR2CN0\_TF2LEN\_\_SHIFT EQU 005H ; Timer 2 Low Byte Interrupt Enable

TMR2CN0\_TF2LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR2CN0\_TF2LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR2CN0\_TF2L\_\_BMASK EQU 040H ; Timer 2 Low Byte Overflow Flag

TMR2CN0\_TF2L\_\_SHIFT EQU 006H ; Timer 2 Low Byte Overflow Flag

TMR2CN0\_TF2L\_\_NOT\_SET EQU 000H ; Timer 2 low byte did not overflow.

TMR2CN0\_TF2L\_\_SET EQU 040H ; Timer 2 low byte overflowed.

TMR2CN0\_TF2H\_\_BMASK EQU 080H ; Timer 2 High Byte Overflow Flag

TMR2CN0\_TF2H\_\_SHIFT EQU 007H ; Timer 2 High Byte Overflow Flag

TMR2CN0\_TF2H\_\_NOT\_SET EQU 000H ; Timer 2 8-bit high byte or 16-bit value did not

; overflow.

TMR2CN0\_TF2H\_\_SET EQU 080H ; Timer 2 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR2H Enums (Timer 2 High Byte @ 0xCD)

;------------------------------------------------------------------------------

TMR2H\_TMR2H\_\_FMASK EQU 0FFH ; Timer 2 High Byte

TMR2H\_TMR2H\_\_SHIFT EQU 000H ; Timer 2 High Byte

;------------------------------------------------------------------------------

; TMR2L Enums (Timer 2 Low Byte @ 0xCC)

;------------------------------------------------------------------------------

TMR2L\_TMR2L\_\_FMASK EQU 0FFH ; Timer 2 Low Byte

TMR2L\_TMR2L\_\_SHIFT EQU 000H ; Timer 2 Low Byte

;------------------------------------------------------------------------------

; TMR2RLH Enums (Timer 2 Reload High Byte @ 0xCB)

;------------------------------------------------------------------------------

TMR2RLH\_TMR2RLH\_\_FMASK EQU 0FFH ; Timer 2 Reload High Byte

TMR2RLH\_TMR2RLH\_\_SHIFT EQU 000H ; Timer 2 Reload High Byte

;------------------------------------------------------------------------------

; TMR2RLL Enums (Timer 2 Reload Low Byte @ 0xCA)

;------------------------------------------------------------------------------

TMR2RLL\_TMR2RLL\_\_FMASK EQU 0FFH ; Timer 2 Reload Low Byte

TMR2RLL\_TMR2RLL\_\_SHIFT EQU 000H ; Timer 2 Reload Low Byte

;------------------------------------------------------------------------------

; TMR3CN0 Enums (Timer 3 Control 0 @ 0x91)

;------------------------------------------------------------------------------

TMR3CN0\_T3XCLK\_\_BMASK EQU 001H ; Timer 3 External Clock Select

TMR3CN0\_T3XCLK\_\_SHIFT EQU 000H ; Timer 3 External Clock Select

TMR3CN0\_T3XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 3 clock is the system clock divided by 12.

TMR3CN0\_T3XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 3 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK).

TMR3CN0\_T3CSS\_\_BMASK EQU 002H ; Timer 3 Capture Source Select

TMR3CN0\_T3CSS\_\_SHIFT EQU 001H ; Timer 3 Capture Source Select

TMR3CN0\_T3CSS\_\_USB\_SOF\_CAPTURE EQU 000H ; Capture source is USB SOF event.

TMR3CN0\_T3CSS\_\_LFOSC\_CAPTURE EQU 002H ; Capture source is falling edge of Low-Frequency

; Oscillator.

TMR3CN0\_TR3\_\_BMASK EQU 004H ; Timer 3 Run Control

TMR3CN0\_TR3\_\_SHIFT EQU 002H ; Timer 3 Run Control

TMR3CN0\_TR3\_\_STOP EQU 000H ; Stop Timer 3.

TMR3CN0\_TR3\_\_RUN EQU 004H ; Start Timer 3 running.

TMR3CN0\_T3SPLIT\_\_BMASK EQU 008H ; Timer 3 Split Mode Enable

TMR3CN0\_T3SPLIT\_\_SHIFT EQU 003H ; Timer 3 Split Mode Enable

TMR3CN0\_T3SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 3 operates in 16-bit auto-reload mode.

TMR3CN0\_T3SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 3 operates as two 8-bit auto-reload timers.

TMR3CN0\_TF3CEN\_\_BMASK EQU 010H ; Timer 3 Capture Enable

TMR3CN0\_TF3CEN\_\_SHIFT EQU 004H ; Timer 3 Capture Enable

TMR3CN0\_TF3CEN\_\_DISABLED EQU 000H ; Disable capture mode.

TMR3CN0\_TF3CEN\_\_ENABLED EQU 010H ; Enable capture mode.

TMR3CN0\_TF3LEN\_\_BMASK EQU 020H ; Timer 3 Low Byte Interrupt Enable

TMR3CN0\_TF3LEN\_\_SHIFT EQU 005H ; Timer 3 Low Byte Interrupt Enable

TMR3CN0\_TF3LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR3CN0\_TF3LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR3CN0\_TF3L\_\_BMASK EQU 040H ; Timer 3 Low Byte Overflow Flag

TMR3CN0\_TF3L\_\_SHIFT EQU 006H ; Timer 3 Low Byte Overflow Flag

TMR3CN0\_TF3L\_\_NOT\_SET EQU 000H ; Timer 3 low byte did not overflow.

TMR3CN0\_TF3L\_\_SET EQU 040H ; Timer 3 low byte overflowed.

TMR3CN0\_TF3H\_\_BMASK EQU 080H ; Timer 3 High Byte Overflow Flag

TMR3CN0\_TF3H\_\_SHIFT EQU 007H ; Timer 3 High Byte Overflow Flag

TMR3CN0\_TF3H\_\_NOT\_SET EQU 000H ; Timer 3 8-bit high byte or 16-bit value did not

; overflow.

TMR3CN0\_TF3H\_\_SET EQU 080H ; Timer 3 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR3H Enums (Timer 3 High Byte @ 0x95)

;------------------------------------------------------------------------------

TMR3H\_TMR3H\_\_FMASK EQU 0FFH ; Timer 3 High Byte

TMR3H\_TMR3H\_\_SHIFT EQU 000H ; Timer 3 High Byte

;------------------------------------------------------------------------------

; TMR3L Enums (Timer 3 Low Byte @ 0x94)

;------------------------------------------------------------------------------

TMR3L\_TMR3L\_\_FMASK EQU 0FFH ; Timer 3 Low Byte

TMR3L\_TMR3L\_\_SHIFT EQU 000H ; Timer 3 Low Byte

;------------------------------------------------------------------------------

; TMR3RLH Enums (Timer 3 Reload High Byte @ 0x93)

;------------------------------------------------------------------------------

TMR3RLH\_TMR3RLH\_\_FMASK EQU 0FFH ; Timer 3 Reload High Byte

TMR3RLH\_TMR3RLH\_\_SHIFT EQU 000H ; Timer 3 Reload High Byte

;------------------------------------------------------------------------------

; TMR3RLL Enums (Timer 3 Reload Low Byte @ 0x92)

;------------------------------------------------------------------------------

TMR3RLL\_TMR3RLL\_\_FMASK EQU 0FFH ; Timer 3 Reload Low Byte

TMR3RLL\_TMR3RLL\_\_SHIFT EQU 000H ; Timer 3 Reload Low Byte

;------------------------------------------------------------------------------

; TMR4CN0 Enums (Timer 4 Control 0 @ 0x91)

;------------------------------------------------------------------------------

TMR4CN0\_T4XCLK\_\_BMASK EQU 001H ; Timer 4 External Clock Select

TMR4CN0\_T4XCLK\_\_SHIFT EQU 000H ; Timer 4 External Clock Select

TMR4CN0\_T4XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 4 clock is the system clock divided by 12.

TMR4CN0\_T4XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 4 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK).

TMR4CN0\_TR4\_\_BMASK EQU 004H ; Timer 4 Run Control

TMR4CN0\_TR4\_\_SHIFT EQU 002H ; Timer 4 Run Control

TMR4CN0\_TR4\_\_STOP EQU 000H ; Stop Timer 4.

TMR4CN0\_TR4\_\_RUN EQU 004H ; Start Timer 4 running.

TMR4CN0\_T4SPLIT\_\_BMASK EQU 008H ; Timer 4 Split Mode Enable

TMR4CN0\_T4SPLIT\_\_SHIFT EQU 003H ; Timer 4 Split Mode Enable

TMR4CN0\_T4SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 4 operates in 16-bit auto-reload mode.

TMR4CN0\_T4SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 4 operates as two 8-bit auto-reload timers.

TMR4CN0\_TF4LEN\_\_BMASK EQU 020H ; Timer 4 Low Byte Interrupt Enable

TMR4CN0\_TF4LEN\_\_SHIFT EQU 005H ; Timer 4 Low Byte Interrupt Enable

TMR4CN0\_TF4LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR4CN0\_TF4LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR4CN0\_TF4L\_\_BMASK EQU 040H ; Timer 4 Low Byte Overflow Flag

TMR4CN0\_TF4L\_\_SHIFT EQU 006H ; Timer 4 Low Byte Overflow Flag

TMR4CN0\_TF4L\_\_NOT\_SET EQU 000H ; Timer 4 low byte did not overflow.

TMR4CN0\_TF4L\_\_SET EQU 040H ; Timer 4 low byte overflowed.

TMR4CN0\_TF4H\_\_BMASK EQU 080H ; Timer 4 High Byte Overflow Flag

TMR4CN0\_TF4H\_\_SHIFT EQU 007H ; Timer 4 High Byte Overflow Flag

TMR4CN0\_TF4H\_\_NOT\_SET EQU 000H ; Timer 4 8-bit high byte or 16-bit value did not

; overflow.

TMR4CN0\_TF4H\_\_SET EQU 080H ; Timer 4 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR4H Enums (Timer 4 High Byte @ 0x95)

;------------------------------------------------------------------------------

TMR4H\_TMR4H\_\_FMASK EQU 0FFH ; Timer 4 High Byte

TMR4H\_TMR4H\_\_SHIFT EQU 000H ; Timer 4 High Byte

;------------------------------------------------------------------------------

; TMR4L Enums (Timer 4 Low Byte @ 0x94)

;------------------------------------------------------------------------------

TMR4L\_TMR4L\_\_FMASK EQU 0FFH ; Timer 4 Low Byte

TMR4L\_TMR4L\_\_SHIFT EQU 000H ; Timer 4 Low Byte

;------------------------------------------------------------------------------

; TMR4RLH Enums (Timer 4 Reload High Byte @ 0x93)

;------------------------------------------------------------------------------

TMR4RLH\_TMR4RLH\_\_FMASK EQU 0FFH ; Timer 4 Reload High Byte

TMR4RLH\_TMR4RLH\_\_SHIFT EQU 000H ; Timer 4 Reload High Byte

;------------------------------------------------------------------------------

; TMR4RLL Enums (Timer 4 Reload Low Byte @ 0x92)

;------------------------------------------------------------------------------

TMR4RLL\_TMR4RLL\_\_FMASK EQU 0FFH ; Timer 4 Reload Low Byte

TMR4RLL\_TMR4RLL\_\_SHIFT EQU 000H ; Timer 4 Reload Low Byte

;------------------------------------------------------------------------------

; TMR5CN0 Enums (Timer 5 Control 0 @ 0xC8)

;------------------------------------------------------------------------------

TMR5CN0\_T5XCLK\_\_BMASK EQU 001H ; Timer 5 External Clock Select

TMR5CN0\_T5XCLK\_\_SHIFT EQU 000H ; Timer 5 External Clock Select

TMR5CN0\_T5XCLK\_\_SYSCLK\_DIV\_12 EQU 000H ; Timer 5 clock is the system clock divided by 12.

TMR5CN0\_T5XCLK\_\_EXTOSC\_DIV\_8 EQU 001H ; Timer 5 clock is the external oscillator divided

; by 8 (synchronized with SYSCLK).

TMR5CN0\_TR5\_\_BMASK EQU 004H ; Timer 5 Run Control

TMR5CN0\_TR5\_\_SHIFT EQU 002H ; Timer 5 Run Control

TMR5CN0\_TR5\_\_STOP EQU 000H ; Stop Timer 5.

TMR5CN0\_TR5\_\_RUN EQU 004H ; Start Timer 5 running.

TMR5CN0\_T5SPLIT\_\_BMASK EQU 008H ; Timer 5 Split Mode Enable

TMR5CN0\_T5SPLIT\_\_SHIFT EQU 003H ; Timer 5 Split Mode Enable

TMR5CN0\_T5SPLIT\_\_16\_BIT\_RELOAD EQU 000H ; Timer 5 operates in 16-bit auto-reload mode.

TMR5CN0\_T5SPLIT\_\_8\_BIT\_RELOAD EQU 008H ; Timer 5 operates as two 8-bit auto-reload timers.

TMR5CN0\_TF5LEN\_\_BMASK EQU 020H ; Timer 5 Low Byte Interrupt Enable

TMR5CN0\_TF5LEN\_\_SHIFT EQU 005H ; Timer 5 Low Byte Interrupt Enable

TMR5CN0\_TF5LEN\_\_DISABLED EQU 000H ; Disable low byte interrupts.

TMR5CN0\_TF5LEN\_\_ENABLED EQU 020H ; Enable low byte interrupts.

TMR5CN0\_TF5L\_\_BMASK EQU 040H ; Timer 5 Low Byte Overflow Flag

TMR5CN0\_TF5L\_\_SHIFT EQU 006H ; Timer 5 Low Byte Overflow Flag

TMR5CN0\_TF5L\_\_NOT\_SET EQU 000H ; Timer 5 low byte did not overflow.

TMR5CN0\_TF5L\_\_SET EQU 040H ; Timer 5 low byte overflowed.

TMR5CN0\_TF5H\_\_BMASK EQU 080H ; Timer 5 High Byte Overflow Flag

TMR5CN0\_TF5H\_\_SHIFT EQU 007H ; Timer 5 High Byte Overflow Flag

TMR5CN0\_TF5H\_\_NOT\_SET EQU 000H ; Timer 5 8-bit high byte or 16-bit value did not

; overflow.

TMR5CN0\_TF5H\_\_SET EQU 080H ; Timer 5 8-bit high byte or 16-bit value

; overflowed.

;------------------------------------------------------------------------------

; TMR5H Enums (Timer 5 High Byte @ 0xCD)

;------------------------------------------------------------------------------

TMR5H\_TMR5H\_\_FMASK EQU 0FFH ; Timer 5 High Byte

TMR5H\_TMR5H\_\_SHIFT EQU 000H ; Timer 5 High Byte

;------------------------------------------------------------------------------

; TMR5L Enums (Timer 5 Low Byte @ 0xCC)

;------------------------------------------------------------------------------

TMR5L\_TMR5L\_\_FMASK EQU 0FFH ; Timer 5 Low Byte

TMR5L\_TMR5L\_\_SHIFT EQU 000H ; Timer 5 Low Byte

;------------------------------------------------------------------------------

; TMR5RLH Enums (Timer 5 Reload High Byte @ 0xCB)

;------------------------------------------------------------------------------

TMR5RLH\_TMR5RLH\_\_FMASK EQU 0FFH ; Timer 5 Reload High Byte

TMR5RLH\_TMR5RLH\_\_SHIFT EQU 000H ; Timer 5 Reload High Byte

;------------------------------------------------------------------------------

; TMR5RLL Enums (Timer 5 Reload Low Byte @ 0xCA)

;------------------------------------------------------------------------------

TMR5RLL\_TMR5RLL\_\_FMASK EQU 0FFH ; Timer 5 Reload Low Byte

TMR5RLL\_TMR5RLL\_\_SHIFT EQU 000H ; Timer 5 Reload Low Byte

;------------------------------------------------------------------------------

; CKCON0 Enums (Clock Control 0 @ 0x8E)

;------------------------------------------------------------------------------

CKCON0\_SCA\_\_FMASK EQU 003H ; Timer 0/1 Prescale

CKCON0\_SCA\_\_SHIFT EQU 000H ; Timer 0/1 Prescale

CKCON0\_SCA\_\_SYSCLK\_DIV\_12 EQU 000H ; System clock divided by 12.

CKCON0\_SCA\_\_SYSCLK\_DIV\_4 EQU 001H ; System clock divided by 4.

CKCON0\_SCA\_\_SYSCLK\_DIV\_48 EQU 002H ; System clock divided by 48.

CKCON0\_SCA\_\_EXTOSC\_DIV\_8 EQU 003H ; External oscillator divided by 8 (synchronized

; with the system clock).

CKCON0\_T0M\_\_BMASK EQU 004H ; Timer 0 Clock Select

CKCON0\_T0M\_\_SHIFT EQU 002H ; Timer 0 Clock Select

CKCON0\_T0M\_\_PRESCALE EQU 000H ; Counter/Timer 0 uses the clock defined by the

; prescale field, SCA.

CKCON0\_T0M\_\_SYSCLK EQU 004H ; Counter/Timer 0 uses the system clock.

CKCON0\_T1M\_\_BMASK EQU 008H ; Timer 1 Clock Select

CKCON0\_T1M\_\_SHIFT EQU 003H ; Timer 1 Clock Select

CKCON0\_T1M\_\_PRESCALE EQU 000H ; Timer 1 uses the clock defined by the prescale

; field, SCA.

CKCON0\_T1M\_\_SYSCLK EQU 008H ; Timer 1 uses the system clock.

CKCON0\_T2ML\_\_BMASK EQU 010H ; Timer 2 Low Byte Clock Select

CKCON0\_T2ML\_\_SHIFT EQU 004H ; Timer 2 Low Byte Clock Select

CKCON0\_T2ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 2 low byte uses the clock defined by T2XCLK

; in TMR2CN0.

CKCON0\_T2ML\_\_SYSCLK EQU 010H ; Timer 2 low byte uses the system clock.

CKCON0\_T2MH\_\_BMASK EQU 020H ; Timer 2 High Byte Clock Select

CKCON0\_T2MH\_\_SHIFT EQU 005H ; Timer 2 High Byte Clock Select

CKCON0\_T2MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 2 high byte uses the clock defined by T2XCLK

; in TMR2CN0.

CKCON0\_T2MH\_\_SYSCLK EQU 020H ; Timer 2 high byte uses the system clock.

CKCON0\_T3ML\_\_BMASK EQU 040H ; Timer 3 Low Byte Clock Select

CKCON0\_T3ML\_\_SHIFT EQU 006H ; Timer 3 Low Byte Clock Select

CKCON0\_T3ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 3 low byte uses the clock defined by T3XCLK

; in TMR3CN0.

CKCON0\_T3ML\_\_SYSCLK EQU 040H ; Timer 3 low byte uses the system clock.

CKCON0\_T3MH\_\_BMASK EQU 080H ; Timer 3 High Byte Clock Select

CKCON0\_T3MH\_\_SHIFT EQU 007H ; Timer 3 High Byte Clock Select

CKCON0\_T3MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 3 high byte uses the clock defined by T3XCLK

; in TMR3CN0.

CKCON0\_T3MH\_\_SYSCLK EQU 080H ; Timer 3 high byte uses the system clock.

;------------------------------------------------------------------------------

; CKCON1 Enums (Clock Control 1 @ 0xE4)

;------------------------------------------------------------------------------

CKCON1\_T4ML\_\_BMASK EQU 001H ; Timer 4 Low Byte Clock Select

CKCON1\_T4ML\_\_SHIFT EQU 000H ; Timer 4 Low Byte Clock Select

CKCON1\_T4ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 4 low byte uses the clock defined by T4XCLK

; in TMR4CN0.

CKCON1\_T4ML\_\_SYSCLK EQU 001H ; Timer 4 low byte uses the system clock.

CKCON1\_T4MH\_\_BMASK EQU 002H ; Timer 4 High Byte Clock Select

CKCON1\_T4MH\_\_SHIFT EQU 001H ; Timer 4 High Byte Clock Select

CKCON1\_T4MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 4 high byte uses the clock defined by T4XCLK

; in TMR4CN0.

CKCON1\_T4MH\_\_SYSCLK EQU 002H ; Timer 4 high byte uses the system clock.

CKCON1\_T5ML\_\_BMASK EQU 004H ; Timer 5 Low Byte Clock Select

CKCON1\_T5ML\_\_SHIFT EQU 002H ; Timer 5 Low Byte Clock Select

CKCON1\_T5ML\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 5 low byte uses the clock defined by T5XCLK

; in TMR5CN.

CKCON1\_T5ML\_\_SYSCLK EQU 004H ; Timer 5 low byte uses the system clock.

CKCON1\_T5MH\_\_BMASK EQU 008H ; Timer 5 High Byte Clock Select

CKCON1\_T5MH\_\_SHIFT EQU 003H ; Timer 5 High Byte Clock Select

CKCON1\_T5MH\_\_EXTERNAL\_CLOCK EQU 000H ; Timer 5 high byte uses the clock defined by T5XCLK

; in TMR5CN.

CKCON1\_T5MH\_\_SYSCLK EQU 008H ; Timer 5 high byte uses the system clock.

;------------------------------------------------------------------------------

; TCON Enums (Timer 0/1 Control @ 0x88)

;------------------------------------------------------------------------------

TCON\_IT0\_\_BMASK EQU 001H ; Interrupt 0 Type Select

TCON\_IT0\_\_SHIFT EQU 000H ; Interrupt 0 Type Select

TCON\_IT0\_\_LEVEL EQU 000H ; INT0 is level triggered.

TCON\_IT0\_\_EDGE EQU 001H ; INT0 is edge triggered.

TCON\_IE0\_\_BMASK EQU 002H ; External Interrupt 0

TCON\_IE0\_\_SHIFT EQU 001H ; External Interrupt 0

TCON\_IE0\_\_NOT\_SET EQU 000H ; Edge/level not detected.

TCON\_IE0\_\_SET EQU 002H ; Edge/level detected

TCON\_IT1\_\_BMASK EQU 004H ; Interrupt 1 Type Select

TCON\_IT1\_\_SHIFT EQU 002H ; Interrupt 1 Type Select

TCON\_IT1\_\_LEVEL EQU 000H ; INT1 is level triggered.

TCON\_IT1\_\_EDGE EQU 004H ; INT1 is edge triggered.

TCON\_IE1\_\_BMASK EQU 008H ; External Interrupt 1

TCON\_IE1\_\_SHIFT EQU 003H ; External Interrupt 1

TCON\_IE1\_\_NOT\_SET EQU 000H ; Edge/level not detected.

TCON\_IE1\_\_SET EQU 008H ; Edge/level detected

TCON\_TR0\_\_BMASK EQU 010H ; Timer 0 Run Control

TCON\_TR0\_\_SHIFT EQU 004H ; Timer 0 Run Control

TCON\_TR0\_\_STOP EQU 000H ; Stop Timer 0.

TCON\_TR0\_\_RUN EQU 010H ; Start Timer 0 running.

TCON\_TF0\_\_BMASK EQU 020H ; Timer 0 Overflow Flag

TCON\_TF0\_\_SHIFT EQU 005H ; Timer 0 Overflow Flag

TCON\_TF0\_\_NOT\_SET EQU 000H ; Timer 0 did not overflow.

TCON\_TF0\_\_SET EQU 020H ; Timer 0 overflowed.

TCON\_TR1\_\_BMASK EQU 040H ; Timer 1 Run Control

TCON\_TR1\_\_SHIFT EQU 006H ; Timer 1 Run Control

TCON\_TR1\_\_STOP EQU 000H ; Stop Timer 1.

TCON\_TR1\_\_RUN EQU 040H ; Start Timer 1 running.

TCON\_TF1\_\_BMASK EQU 080H ; Timer 1 Overflow Flag

TCON\_TF1\_\_SHIFT EQU 007H ; Timer 1 Overflow Flag

TCON\_TF1\_\_NOT\_SET EQU 000H ; Timer 1 did not overflow.

TCON\_TF1\_\_SET EQU 080H ; Timer 1 overflowed.

;------------------------------------------------------------------------------

; TMOD Enums (Timer 0/1 Mode @ 0x89)

;------------------------------------------------------------------------------

TMOD\_T0M\_\_FMASK EQU 003H ; Timer 0 Mode Select

TMOD\_T0M\_\_SHIFT EQU 000H ; Timer 0 Mode Select

TMOD\_T0M\_\_MODE0 EQU 000H ; Mode 0, 13-bit Counter/Timer

TMOD\_T0M\_\_MODE1 EQU 001H ; Mode 1, 16-bit Counter/Timer

TMOD\_T0M\_\_MODE2 EQU 002H ; Mode 2, 8-bit Counter/Timer with Auto-Reload

TMOD\_T0M\_\_MODE3 EQU 003H ; Mode 3, Two 8-bit Counter/Timers

TMOD\_CT0\_\_BMASK EQU 004H ; Counter/Timer 0 Select

TMOD\_CT0\_\_SHIFT EQU 002H ; Counter/Timer 0 Select

TMOD\_CT0\_\_TIMER EQU 000H ; Timer Mode. Timer 0 increments on the clock

; defined by T0M in the CKCON0 register.

TMOD\_CT0\_\_COUNTER EQU 004H ; Counter Mode. Timer 0 increments on high-to-low

; transitions of an external pin (T0).

TMOD\_GATE0\_\_BMASK EQU 008H ; Timer 0 Gate Control

TMOD\_GATE0\_\_SHIFT EQU 003H ; Timer 0 Gate Control

TMOD\_GATE0\_\_DISABLED EQU 000H ; Timer 0 enabled when TR0 = 1 irrespective of INT0

; logic level.

TMOD\_GATE0\_\_ENABLED EQU 008H ; Timer 0 enabled only when TR0 = 1 and INT0 is

; active as defined by bit IN0PL in register IT01CF.

TMOD\_T1M\_\_FMASK EQU 030H ; Timer 1 Mode Select

TMOD\_T1M\_\_SHIFT EQU 004H ; Timer 1 Mode Select

TMOD\_T1M\_\_MODE0 EQU 000H ; Mode 0, 13-bit Counter/Timer

TMOD\_T1M\_\_MODE1 EQU 010H ; Mode 1, 16-bit Counter/Timer

TMOD\_T1M\_\_MODE2 EQU 020H ; Mode 2, 8-bit Counter/Timer with Auto-Reload

TMOD\_T1M\_\_MODE3 EQU 030H ; Mode 3, Timer 1 Inactive

TMOD\_CT1\_\_BMASK EQU 040H ; Counter/Timer 1 Select

TMOD\_CT1\_\_SHIFT EQU 006H ; Counter/Timer 1 Select

TMOD\_CT1\_\_TIMER EQU 000H ; Timer Mode. Timer 1 increments on the clock

; defined by T1M in the CKCON0 register.

TMOD\_CT1\_\_COUNTER EQU 040H ; Counter Mode. Timer 1 increments on high-to-low

; transitions of an external pin (T1).

TMOD\_GATE1\_\_BMASK EQU 080H ; Timer 1 Gate Control

TMOD\_GATE1\_\_SHIFT EQU 007H ; Timer 1 Gate Control

TMOD\_GATE1\_\_DISABLED EQU 000H ; Timer 1 enabled when TR1 = 1 irrespective of INT1

; logic level.

TMOD\_GATE1\_\_ENABLED EQU 080H ; Timer 1 enabled only when TR1 = 1 and INT1 is

; active as defined by bit IN1PL in register IT01CF.

;------------------------------------------------------------------------------

; SBCON1 Enums (UART1 Baud Rate Generator Control @ 0xAC)

;------------------------------------------------------------------------------

SBCON1\_BPS\_\_FMASK EQU 003H ; Baud Rate Prescaler Select

SBCON1\_BPS\_\_SHIFT EQU 000H ; Baud Rate Prescaler Select

SBCON1\_BPS\_\_DIV\_BY\_12 EQU 000H ; Prescaler = 12.

SBCON1\_BPS\_\_DIV\_BY\_4 EQU 001H ; Prescaler = 4.

SBCON1\_BPS\_\_DIV\_BY\_48 EQU 002H ; Prescaler = 48.

SBCON1\_BPS\_\_DIV\_BY\_1 EQU 003H ; Prescaler = 1.

SBCON1\_BREN\_\_BMASK EQU 040H ; Baud Rate Generator Enable

SBCON1\_BREN\_\_SHIFT EQU 006H ; Baud Rate Generator Enable

SBCON1\_BREN\_\_DISABLED EQU 000H ; Disable the baud rate generator. UART1 will not

; function.

SBCON1\_BREN\_\_ENABLED EQU 040H ; Enable the baud rate generator.

;------------------------------------------------------------------------------

; SBRLH1 Enums (UART1 Baud Rate Generator High Byte @ 0xB5)

;------------------------------------------------------------------------------

SBRLH1\_BRH\_\_FMASK EQU 0FFH ; UART1 Baud Rate Reload High

SBRLH1\_BRH\_\_SHIFT EQU 000H ; UART1 Baud Rate Reload High

;------------------------------------------------------------------------------

; SBRLL1 Enums (UART1 Baud Rate Generator Low Byte @ 0xB4)

;------------------------------------------------------------------------------

SBRLL1\_BRL\_\_FMASK EQU 0FFH ; UART1 Baud Rate Reload Low

SBRLL1\_BRL\_\_SHIFT EQU 000H ; UART1 Baud Rate Reload Low

;------------------------------------------------------------------------------

; SBUF1 Enums (UART1 Serial Port Data Buffer @ 0xD3)

;------------------------------------------------------------------------------

SBUF1\_SBUF1\_\_FMASK EQU 0FFH ; Serial Port Data Buffer

SBUF1\_SBUF1\_\_SHIFT EQU 000H ; Serial Port Data Buffer

;------------------------------------------------------------------------------

; SCON1 Enums (UART1 Serial Port Control @ 0xD2)

;------------------------------------------------------------------------------

SCON1\_RI\_\_BMASK EQU 001H ; Receive Interrupt Flag

SCON1\_RI\_\_SHIFT EQU 000H ; Receive Interrupt Flag

SCON1\_RI\_\_NOT\_SET EQU 000H ; New data has not been received by UART1.

SCON1\_RI\_\_SET EQU 001H ; UART1 received one or more data bytes.

SCON1\_TI\_\_BMASK EQU 002H ; Transmit Interrupt Flag

SCON1\_TI\_\_SHIFT EQU 001H ; Transmit Interrupt Flag

SCON1\_TI\_\_NOT\_SET EQU 000H ; A byte of data has not been transmitted by UART1.

SCON1\_TI\_\_SET EQU 002H ; UART1 transmitted a byte of data.

SCON1\_RBX\_\_BMASK EQU 004H ; Extra Receive Bit

SCON1\_RBX\_\_SHIFT EQU 002H ; Extra Receive Bit

SCON1\_RBX\_\_LOW EQU 000H ; The extra bit or the first stop bit is 0.

SCON1\_RBX\_\_HIGH EQU 004H ; The extra bit or the first stop bit is 1.

SCON1\_TBX\_\_BMASK EQU 008H ; Extra Transmission Bit

SCON1\_TBX\_\_SHIFT EQU 003H ; Extra Transmission Bit

SCON1\_TBX\_\_LOW EQU 000H ; Set extra bit to 0 (low).

SCON1\_TBX\_\_HIGH EQU 008H ; Set extra bit to 1 (high).

SCON1\_REN\_\_BMASK EQU 010H ; Receive Enable

SCON1\_REN\_\_SHIFT EQU 004H ; Receive Enable

SCON1\_REN\_\_RECEIVE\_DISABLED EQU 000H ; UART1 reception disabled.

SCON1\_REN\_\_RECEIVE\_ENABLED EQU 010H ; UART1 reception enabled.

SCON1\_PERR\_\_BMASK EQU 040H ; Parity Error Flag

SCON1\_PERR\_\_SHIFT EQU 006H ; Parity Error Flag

SCON1\_PERR\_\_NOT\_SET EQU 000H ; Parity error has not occurred.

SCON1\_PERR\_\_SET EQU 040H ; Parity error has occurred.

SCON1\_OVR\_\_BMASK EQU 080H ; Receive FIFO Overrun Flag

SCON1\_OVR\_\_SHIFT EQU 007H ; Receive FIFO Overrun Flag

SCON1\_OVR\_\_NOT\_SET EQU 000H ; Receive FIFO overrun has not occurred.

SCON1\_OVR\_\_SET EQU 080H ; Receive FIFO overrun has occurred.

;------------------------------------------------------------------------------

; SMOD1 Enums (UART1 Mode @ 0xE5)

;------------------------------------------------------------------------------

SMOD1\_SBL\_\_BMASK EQU 001H ; Stop Bit Length

SMOD1\_SBL\_\_SHIFT EQU 000H ; Stop Bit Length

SMOD1\_SBL\_\_SHORT EQU 000H ; Short: Stop bit is active for one bit time.

SMOD1\_SBL\_\_LONG EQU 001H ; Long: Stop bit is active for two bit times (data

; length = 6, 7, or 8 bits) or 1.5 bit times (data

; length = 5 bits).

SMOD1\_XBE\_\_BMASK EQU 002H ; Extra Bit Enable

SMOD1\_XBE\_\_SHIFT EQU 001H ; Extra Bit Enable

SMOD1\_XBE\_\_DISABLED EQU 000H ; Disable the extra bit.

SMOD1\_XBE\_\_ENABLED EQU 002H ; Enable the extra bit.

SMOD1\_SDL\_\_FMASK EQU 00CH ; Data Length

SMOD1\_SDL\_\_SHIFT EQU 002H ; Data Length

SMOD1\_SDL\_\_5\_BITS EQU 000H ; 5 bits.

SMOD1\_SDL\_\_6\_BITS EQU 004H ; 6 bits.

SMOD1\_SDL\_\_7\_BITS EQU 008H ; 7 bits.

SMOD1\_SDL\_\_8\_BITS EQU 00CH ; 8 bits.

SMOD1\_PE\_\_BMASK EQU 010H ; Parity Enable

SMOD1\_PE\_\_SHIFT EQU 004H ; Parity Enable

SMOD1\_PE\_\_PARITY\_DISABLED EQU 000H ; Disable hardware parity.

SMOD1\_PE\_\_PARITY\_ENABLED EQU 010H ; Enable hardware parity.

SMOD1\_SPT\_\_FMASK EQU 060H ; Parity Type

SMOD1\_SPT\_\_SHIFT EQU 005H ; Parity Type

SMOD1\_SPT\_\_ODD\_PARTY EQU 000H ; Odd.

SMOD1\_SPT\_\_EVEN\_PARITY EQU 020H ; Even.

SMOD1\_SPT\_\_MARK\_PARITY EQU 040H ; Mark.

SMOD1\_SPT\_\_SPACE\_PARITY EQU 060H ; Space.

SMOD1\_MCE\_\_BMASK EQU 080H ; Multiprocessor Communication Enable

SMOD1\_MCE\_\_SHIFT EQU 007H ; Multiprocessor Communication Enable

SMOD1\_MCE\_\_MULTI\_DISABLED EQU 000H ; RI will be activated if the stop bits are 1.

SMOD1\_MCE\_\_MULTI\_ENABLED EQU 080H ; RI will be activated if the stop bits and extra

; bit are 1. The extra bit must be enabled using

; XBE.

;------------------------------------------------------------------------------

; SBUF0 Enums (UART0 Serial Port Data Buffer @ 0x99)

;------------------------------------------------------------------------------

SBUF0\_SBUF0\_\_FMASK EQU 0FFH ; Serial Data Buffer

SBUF0\_SBUF0\_\_SHIFT EQU 000H ; Serial Data Buffer

;------------------------------------------------------------------------------

; SCON0 Enums (UART0 Serial Port Control @ 0x98)

;------------------------------------------------------------------------------

SCON0\_RI\_\_BMASK EQU 001H ; Receive Interrupt Flag

SCON0\_RI\_\_SHIFT EQU 000H ; Receive Interrupt Flag

SCON0\_RI\_\_NOT\_SET EQU 000H ; A byte of data has not been received by UART0.

SCON0\_RI\_\_SET EQU 001H ; UART0 received a byte of data.

SCON0\_TI\_\_BMASK EQU 002H ; Transmit Interrupt Flag

SCON0\_TI\_\_SHIFT EQU 001H ; Transmit Interrupt Flag

SCON0\_TI\_\_NOT\_SET EQU 000H ; A byte of data has not been transmitted by UART0.

SCON0\_TI\_\_SET EQU 002H ; UART0 transmitted a byte of data.

SCON0\_RB8\_\_BMASK EQU 004H ; Ninth Receive Bit

SCON0\_RB8\_\_SHIFT EQU 002H ; Ninth Receive Bit

SCON0\_RB8\_\_CLEARED\_TO\_0 EQU 000H ; In Mode 0, the STOP bit was 0. In Mode 1, the 9th

; bit was 0.

SCON0\_RB8\_\_SET\_TO\_1 EQU 004H ; In Mode 0, the STOP bit was 1. In Mode 1, the 9th

; bit was 1.

SCON0\_TB8\_\_BMASK EQU 008H ; Ninth Transmission Bit

SCON0\_TB8\_\_SHIFT EQU 003H ; Ninth Transmission Bit

SCON0\_TB8\_\_CLEARED\_TO\_0 EQU 000H ; In Mode 1, set the 9th transmission bit to 0.

SCON0\_TB8\_\_SET\_TO\_1 EQU 008H ; In Mode 1, set the 9th transmission bit to 1.

SCON0\_REN\_\_BMASK EQU 010H ; Receive Enable

SCON0\_REN\_\_SHIFT EQU 004H ; Receive Enable

SCON0\_REN\_\_RECEIVE\_DISABLED EQU 000H ; UART0 reception disabled.

SCON0\_REN\_\_RECEIVE\_ENABLED EQU 010H ; UART0 reception enabled.

SCON0\_MCE\_\_BMASK EQU 020H ; Multiprocessor Communication Enable

SCON0\_MCE\_\_SHIFT EQU 005H ; Multiprocessor Communication Enable

SCON0\_MCE\_\_MULTI\_DISABLED EQU 000H ; Ignore level of 9th bit / Stop bit.

SCON0\_MCE\_\_MULTI\_ENABLED EQU 020H ; RI is set and an interrupt is generated only when

; the stop bit is logic 1 (Mode 0) or when the 9th

; bit is logic 1 (Mode 1).

SCON0\_SMODE\_\_BMASK EQU 080H ; Serial Port 0 Operation Mode

SCON0\_SMODE\_\_SHIFT EQU 007H ; Serial Port 0 Operation Mode

SCON0\_SMODE\_\_8\_BIT EQU 000H ; 8-bit UART with Variable Baud Rate (Mode 0).

SCON0\_SMODE\_\_9\_BIT EQU 080H ; 9-bit UART with Variable Baud Rate (Mode 1).

;------------------------------------------------------------------------------

; CLKREC Enums (USB0 Clock Recovery Control @ 0x0F)

;------------------------------------------------------------------------------

CLKREC\_CRLOW\_\_BMASK EQU 020H ; Low Speed Clock Recovery Mode

CLKREC\_CRLOW\_\_SHIFT EQU 005H ; Low Speed Clock Recovery Mode

CLKREC\_CRLOW\_\_FULL\_SPEED EQU 000H ; Full Speed Mode.

CLKREC\_CRLOW\_\_LOW\_SPEED EQU 020H ; Low Speed Mode.

CLKREC\_CRSSEN\_\_BMASK EQU 040H ; Clock Recovery Single Step

CLKREC\_CRSSEN\_\_SHIFT EQU 006H ; Clock Recovery Single Step

CLKREC\_CRSSEN\_\_DISABLED EQU 000H ; Disable single-step mode (normal calibration

; mode).

CLKREC\_CRSSEN\_\_ENABLED EQU 040H ; Enable single-step mode.

CLKREC\_CRE\_\_BMASK EQU 080H ; Clock Recovery Enable

CLKREC\_CRE\_\_SHIFT EQU 007H ; Clock Recovery Enable

CLKREC\_CRE\_\_DISABLED EQU 000H ; Disable clock recovery.

CLKREC\_CRE\_\_ENABLED EQU 080H ; Enable clock recovery.

;------------------------------------------------------------------------------

; CMIE Enums (USB0 Common Interrupt Enable @ 0x0B)

;------------------------------------------------------------------------------

CMIE\_SUSINTE\_\_BMASK EQU 001H ; Suspend Interrupt Enable

CMIE\_SUSINTE\_\_SHIFT EQU 000H ; Suspend Interrupt Enable

CMIE\_SUSINTE\_\_DISABLED EQU 000H ; Disable suspend interrupts.

CMIE\_SUSINTE\_\_ENABLED EQU 001H ; Enable suspend interrupts.

CMIE\_RSUINTE\_\_BMASK EQU 002H ; Resume Interrupt Enable

CMIE\_RSUINTE\_\_SHIFT EQU 001H ; Resume Interrupt Enable

CMIE\_RSUINTE\_\_DISABLED EQU 000H ; Disable resume interrupts.

CMIE\_RSUINTE\_\_ENABLED EQU 002H ; Enable resume interrupts.

CMIE\_RSTINTE\_\_BMASK EQU 004H ; Reset Interrupt Enable

CMIE\_RSTINTE\_\_SHIFT EQU 002H ; Reset Interrupt Enable

CMIE\_RSTINTE\_\_DISABLED EQU 000H ; Disable reset interrupts.

CMIE\_RSTINTE\_\_ENABLED EQU 004H ; Enable reset interrupts.

CMIE\_SOFE\_\_BMASK EQU 008H ; Start of Frame Interrupt Enable

CMIE\_SOFE\_\_SHIFT EQU 003H ; Start of Frame Interrupt Enable

CMIE\_SOFE\_\_DISABLED EQU 000H ; Disable SOF interrupts.

CMIE\_SOFE\_\_ENABLED EQU 008H ; Enable SOF interrupts.

;------------------------------------------------------------------------------

; CMINT Enums (USB0 Common Interrupt @ 0x06)

;------------------------------------------------------------------------------

CMINT\_SUSINT\_\_BMASK EQU 001H ; Suspend Interrupt Flag

CMINT\_SUSINT\_\_SHIFT EQU 000H ; Suspend Interrupt Flag

CMINT\_SUSINT\_\_NOT\_SET EQU 000H ; Suspend interrupt inactive.

CMINT\_SUSINT\_\_SET EQU 001H ; Suspend interrupt active.

CMINT\_RSUINT\_\_BMASK EQU 002H ; Resume Interrupt Flag

CMINT\_RSUINT\_\_SHIFT EQU 001H ; Resume Interrupt Flag

CMINT\_RSUINT\_\_NOT\_SET EQU 000H ; Resume interrupt inactive.

CMINT\_RSUINT\_\_SET EQU 002H ; Resume interrupt active.

CMINT\_RSTINT\_\_BMASK EQU 004H ; Reset Interrupt Flag

CMINT\_RSTINT\_\_SHIFT EQU 002H ; Reset Interrupt Flag

CMINT\_RSTINT\_\_NOT\_SET EQU 000H ; Reset interrupt inactive.

CMINT\_RSTINT\_\_SET EQU 004H ; Reset interrupt active.

CMINT\_SOF\_\_BMASK EQU 008H ; Start of Frame Interrupt Flag

CMINT\_SOF\_\_SHIFT EQU 003H ; Start of Frame Interrupt Flag

CMINT\_SOF\_\_NOT\_SET EQU 000H ; SOF interrupt inactive.

CMINT\_SOF\_\_SET EQU 008H ; SOF interrupt active.

;------------------------------------------------------------------------------

; E0CNT Enums (USB0 Endpoint0 Data Count @ 0x16)

;------------------------------------------------------------------------------

E0CNT\_E0CNT\_\_FMASK EQU 07FH ; Endpoint 0 Data Count

E0CNT\_E0CNT\_\_SHIFT EQU 000H ; Endpoint 0 Data Count

;------------------------------------------------------------------------------

; E0CSR Enums (USB0 Endpoint0 Control @ 0x11)

;------------------------------------------------------------------------------

E0CSR\_OPRDY\_\_BMASK EQU 001H ; OUT Packet Ready

E0CSR\_OPRDY\_\_SHIFT EQU 000H ; OUT Packet Ready

E0CSR\_OPRDY\_\_NOT\_SET EQU 000H ; A data packet has not been received.

E0CSR\_OPRDY\_\_SET EQU 001H ; A data packet has been received.

E0CSR\_INPRDY\_\_BMASK EQU 002H ; IN Packet Ready

E0CSR\_INPRDY\_\_SHIFT EQU 001H ; IN Packet Ready

E0CSR\_INPRDY\_\_NOT\_SET EQU 000H ; An IN packet is not ready to transmit.

E0CSR\_INPRDY\_\_SET EQU 002H ; An IN packet is ready to transmit.

E0CSR\_STSTL\_\_BMASK EQU 004H ; Sent Stall

E0CSR\_STSTL\_\_SHIFT EQU 002H ; Sent Stall

E0CSR\_STSTL\_\_NOT\_SET EQU 000H ; A STALL handshake signal was not transmitted.

E0CSR\_STSTL\_\_SET EQU 004H ; A STALL handshake signal was transmitted.

E0CSR\_DATAEND\_\_BMASK EQU 008H ; Data End

E0CSR\_DATAEND\_\_SHIFT EQU 003H ; Data End

E0CSR\_DATAEND\_\_NOT\_SET EQU 000H ; This is not the last data packet.

E0CSR\_DATAEND\_\_SET EQU 008H ; This is the last data packet.

E0CSR\_SUEND\_\_BMASK EQU 010H ; Setup End

E0CSR\_SUEND\_\_SHIFT EQU 004H ; Setup End

E0CSR\_SUEND\_\_NOT\_SET EQU 000H ; A control transaction did not end before firmware

; wrote a 1 to the DATAEND bit.

E0CSR\_SUEND\_\_SET EQU 010H ; A control transaction ended before firmware wrote

; a 1 to the DATAEND bit.

E0CSR\_SDSTL\_\_BMASK EQU 020H ; Send Stall

E0CSR\_SDSTL\_\_SHIFT EQU 005H ; Send Stall

E0CSR\_SDSTL\_\_NOT\_SET EQU 000H ; Do not send a STALL.

E0CSR\_SDSTL\_\_SET EQU 020H ; Send a STALL.

E0CSR\_SOPRDY\_\_BMASK EQU 040H ; Serviced OPRDY

E0CSR\_SOPRDY\_\_SHIFT EQU 006H ; Serviced OPRDY

E0CSR\_SOPRDY\_\_NOT\_SET EQU 000H ; OUT packet has not been serviced.

E0CSR\_SOPRDY\_\_SET EQU 040H ; OUT packet has been serviced.

E0CSR\_SSUEND\_\_BMASK EQU 080H ; Serviced Setup End

E0CSR\_SSUEND\_\_SHIFT EQU 007H ; Serviced Setup End

E0CSR\_SSUEND\_\_NOT\_SET EQU 000H ; The setup end (SUEND) event has not been serviced.

E0CSR\_SSUEND\_\_SET EQU 080H ; The setup end (SUEND) event has been serviced.

;------------------------------------------------------------------------------

; EENABLE Enums (USB0 Endpoint Enable @ 0x1E)

;------------------------------------------------------------------------------

EENABLE\_EEN1\_\_BMASK EQU 002H ; Endpoint 1 Enable

EENABLE\_EEN1\_\_SHIFT EQU 001H ; Endpoint 1 Enable

EENABLE\_EEN1\_\_DISABLED EQU 000H ; Disable Endpoint 1 (no NACK, ACK, or STALL on the

; USB network).

EENABLE\_EEN1\_\_ENABLED EQU 002H ; Enable Endpoint 1 (normal).

EENABLE\_EEN2\_\_BMASK EQU 004H ; Endpoint 2 Enable

EENABLE\_EEN2\_\_SHIFT EQU 002H ; Endpoint 2 Enable

EENABLE\_EEN2\_\_DISABLED EQU 000H ; Disable Endpoint 2 (no NACK, ACK, or STALL on the

; USB network).

EENABLE\_EEN2\_\_ENABLED EQU 004H ; Enable Endpoint 2 (normal).

EENABLE\_EEN3\_\_BMASK EQU 008H ; Endpoint 3 Enable

EENABLE\_EEN3\_\_SHIFT EQU 003H ; Endpoint 3 Enable

EENABLE\_EEN3\_\_DISABLED EQU 000H ; Disable Endpoint 3 (no NACK, ACK, or STALL on the

; USB network).

EENABLE\_EEN3\_\_ENABLED EQU 008H ; Enable Endpoint 3 (normal).

;------------------------------------------------------------------------------

; EINCSRH Enums (USB0 IN Endpoint Control High @ 0x12)

;------------------------------------------------------------------------------

EINCSRH\_SPLIT\_\_BMASK EQU 004H ; FIFO Split Enable

EINCSRH\_SPLIT\_\_SHIFT EQU 002H ; FIFO Split Enable

EINCSRH\_SPLIT\_\_DISABLED EQU 000H ; Disable split mode.

EINCSRH\_SPLIT\_\_ENABLED EQU 004H ; Enable split mode.

EINCSRH\_FCDT\_\_BMASK EQU 008H ; Force Data Toggle

EINCSRH\_FCDT\_\_SHIFT EQU 003H ; Force Data Toggle

EINCSRH\_FCDT\_\_ACK\_TOGGLE EQU 000H ; Endpoint data toggle switches only when an ACK is

; received following a data packet transmission.

EINCSRH\_FCDT\_\_ALWAYS\_TOGGLE EQU 008H ; Endpoint data toggle forced to switch after every

; data packet is transmitted, regardless of ACK

; reception.

EINCSRH\_DIRSEL\_\_BMASK EQU 020H ; Endpoint Direction Select

EINCSRH\_DIRSEL\_\_SHIFT EQU 005H ; Endpoint Direction Select

EINCSRH\_DIRSEL\_\_OUT EQU 000H ; Endpoint direction selected as OUT.

EINCSRH\_DIRSEL\_\_IN EQU 020H ; Endpoint direction selected as IN.

EINCSRH\_ISO\_\_BMASK EQU 040H ; Isochronous Transfer Enable

EINCSRH\_ISO\_\_SHIFT EQU 006H ; Isochronous Transfer Enable

EINCSRH\_ISO\_\_DISABLED EQU 000H ; Endpoint configured for Bulk/Interrupt transfers.

EINCSRH\_ISO\_\_ENABLED EQU 040H ; Endpoint configured for Isochronous transfers.

EINCSRH\_DBIEN\_\_BMASK EQU 080H ; IN Endpoint Double-Buffer Enable

EINCSRH\_DBIEN\_\_SHIFT EQU 007H ; IN Endpoint Double-Buffer Enable

EINCSRH\_DBIEN\_\_DISABLED EQU 000H ; Disable double-buffering for the selected IN

; endpoint.

EINCSRH\_DBIEN\_\_ENABLED EQU 080H ; Enable double-buffering for the selected IN

; endpoint.

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; EINCSRL Enums (USB0 IN Endpoint Control Low @ 0x11)

;------------------------------------------------------------------------------

EINCSRL\_INPRDY\_\_BMASK EQU 001H ; In Packet Ready

EINCSRL\_INPRDY\_\_SHIFT EQU 000H ; In Packet Ready

EINCSRL\_INPRDY\_\_NOT\_SET EQU 000H ; A packet is not available in the Endpoint IN FIFO.

EINCSRL\_INPRDY\_\_SET EQU 001H ; A packet is available in the Endpoint IN FIFO.

EINCSRL\_FIFONE\_\_BMASK EQU 002H ; FIFO Not Empty

EINCSRL\_FIFONE\_\_SHIFT EQU 001H ; FIFO Not Empty

EINCSRL\_FIFONE\_\_EMPTY EQU 000H ; The IN Endpoint FIFO is empty.

EINCSRL\_FIFONE\_\_NOT\_EMPTY EQU 002H ; The IN Endpoint FIFO contains one or more packets.

EINCSRL\_UNDRUN\_\_BMASK EQU 004H ; Data Underrun Flag

EINCSRL\_UNDRUN\_\_SHIFT EQU 002H ; Data Underrun Flag

EINCSRL\_UNDRUN\_\_NOT\_SET EQU 000H ; A data underrun did not occur.

EINCSRL\_UNDRUN\_\_SET EQU 004H ; A data underrun occurred.

EINCSRL\_FLUSH\_\_BMASK EQU 008H ; FIFO Flush

EINCSRL\_FLUSH\_\_SHIFT EQU 003H ; FIFO Flush

EINCSRL\_FLUSH\_\_NOT\_SET EQU 000H ; Do not flush the next packet.

EINCSRL\_FLUSH\_\_SET EQU 008H ; Flush the next packet to be transmitted from the

; IN Endpoint FIFO.

EINCSRL\_SDSTL\_\_BMASK EQU 010H ; Send Stall

EINCSRL\_SDSTL\_\_SHIFT EQU 004H ; Send Stall

EINCSRL\_SDSTL\_\_NOT\_SET EQU 000H ; Terminate the STALL.

EINCSRL\_SDSTL\_\_SET EQU 010H ; Generate a STALL in response to an IN token.

EINCSRL\_STSTL\_\_BMASK EQU 020H ; Sent Stall Flag

EINCSRL\_STSTL\_\_SHIFT EQU 005H ; Sent Stall Flag

EINCSRL\_STSTL\_\_NOT\_SET EQU 000H ; A STALL handshake was not transmitted.

EINCSRL\_STSTL\_\_SET EQU 020H ; A STALL handshake was transmitted.

EINCSRL\_CLRDT\_\_BMASK EQU 040H ; Clear Data Toggle

EINCSRL\_CLRDT\_\_SHIFT EQU 006H ; Clear Data Toggle

EINCSRL\_CLRDT\_\_CLEAR EQU 000H ; Clear the IN Endpoint data toggle.

;------------------------------------------------------------------------------

; EOUTCNTH Enums (USB0 OUT Endpoint Count High @ 0x17)

;------------------------------------------------------------------------------

EOUTCNTH\_EOCH\_\_FMASK EQU 003H ; OUT Endpoint Count High

EOUTCNTH\_EOCH\_\_SHIFT EQU 000H ; OUT Endpoint Count High

;------------------------------------------------------------------------------

; EOUTCNTL Enums (USB0 OUT Endpoint Count Low @ 0x16)

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EOUTCNTL\_EOCL\_\_FMASK EQU 0FFH ; OUT Endpoint Count Low

EOUTCNTL\_EOCL\_\_SHIFT EQU 000H ; OUT Endpoint Count Low

;------------------------------------------------------------------------------

; EOUTCSRH Enums (USB0 OUT Endpoint Control High @ 0x15)

;------------------------------------------------------------------------------

EOUTCSRH\_ISO\_\_BMASK EQU 040H ; Isochronous Transfer Enable

EOUTCSRH\_ISO\_\_SHIFT EQU 006H ; Isochronous Transfer Enable

EOUTCSRH\_ISO\_\_DISABLED EQU 000H ; Endpoint configured for Bulk/Interrupt transfers.

EOUTCSRH\_ISO\_\_ENABLED EQU 040H ; Endpoint configured for Isochronous transfers.

EOUTCSRH\_DBOEN\_\_BMASK EQU 080H ; Double-Buffer Enable

EOUTCSRH\_DBOEN\_\_SHIFT EQU 007H ; Double-Buffer Enable

EOUTCSRH\_DBOEN\_\_DISABLED EQU 000H ; Disable double-buffering for the selected OUT

; endpoint.

EOUTCSRH\_DBOEN\_\_ENABLED EQU 080H ; Enable double-buffering for the selected OUT

; endpoint.

;------------------------------------------------------------------------------

; EOUTCSRL Enums (USB0 OUT Endpoint Control Low @ 0x14)

;------------------------------------------------------------------------------

EOUTCSRL\_OPRDY\_\_BMASK EQU 001H ; OUT Packet Ready

EOUTCSRL\_OPRDY\_\_SHIFT EQU 000H ; OUT Packet Ready

EOUTCSRL\_OPRDY\_\_NOT\_SET EQU 000H ; A data packet is not available in the Endpoint OUT

; FIFO.

EOUTCSRL\_OPRDY\_\_SET EQU 001H ; A data packet is available in the Endpoint OUT

; FIFO.

EOUTCSRL\_FIFOFUL\_\_BMASK EQU 002H ; OUT FIFO Full

EOUTCSRL\_FIFOFUL\_\_SHIFT EQU 001H ; OUT FIFO Full

EOUTCSRL\_FIFOFUL\_\_NOT\_FULL EQU 000H ; OUT endpoint FIFO is not full.

EOUTCSRL\_FIFOFUL\_\_FULL EQU 002H ; OUT endpoint FIFO is full.

EOUTCSRL\_OVRUN\_\_BMASK EQU 004H ; Data Overrun Flag

EOUTCSRL\_OVRUN\_\_SHIFT EQU 002H ; Data Overrun Flag

EOUTCSRL\_OVRUN\_\_NOT\_SET EQU 000H ; No data overrun.

EOUTCSRL\_OVRUN\_\_SET EQU 004H ; A data packet was lost because of a full FIFO

; since this flag was last cleared.

EOUTCSRL\_DATERR\_\_BMASK EQU 008H ; Data Error Flag

EOUTCSRL\_DATERR\_\_SHIFT EQU 003H ; Data Error Flag

EOUTCSRL\_DATERR\_\_NOT\_SET EQU 000H ; A received packet does not have a CRC or bit-

; stuffing error.

EOUTCSRL\_DATERR\_\_SET EQU 008H ; A received packet has a CRC or bit-stuffing error.

EOUTCSRL\_FLUSH\_\_BMASK EQU 010H ; FIFO Flush

EOUTCSRL\_FLUSH\_\_SHIFT EQU 004H ; FIFO Flush

EOUTCSRL\_FLUSH\_\_NOT\_SET EQU 000H ; Do not flush the next packet.

EOUTCSRL\_FLUSH\_\_SET EQU 010H ; Flush the next packet to be read from the OUT

; endpoint FIFO.

EOUTCSRL\_SDSTL\_\_BMASK EQU 020H ; Send Stall

EOUTCSRL\_SDSTL\_\_SHIFT EQU 005H ; Send Stall

EOUTCSRL\_SDSTL\_\_NOT\_SET EQU 000H ; Terminate the STALL.

EOUTCSRL\_SDSTL\_\_SET EQU 020H ; Generate a STALL handshake.

EOUTCSRL\_STSTL\_\_BMASK EQU 040H ; Sent Stall Flag

EOUTCSRL\_STSTL\_\_SHIFT EQU 006H ; Sent Stall Flag

EOUTCSRL\_STSTL\_\_NOT\_SET EQU 000H ; A STALL handshake was not transmitted.

EOUTCSRL\_STSTL\_\_SET EQU 040H ; A STALL handshake was transmitted.

EOUTCSRL\_CLRDT\_\_BMASK EQU 080H ; Clear Data Toggle

EOUTCSRL\_CLRDT\_\_SHIFT EQU 007H ; Clear Data Toggle

EOUTCSRL\_CLRDT\_\_CLEAR EQU 000H ; Clear the OUT Endpoint data toggle.

;------------------------------------------------------------------------------

; FADDR Enums (USB0 Function Address @ 0x00)

;------------------------------------------------------------------------------

FADDR\_FADDR\_\_FMASK EQU 07FH ; Function Address

FADDR\_FADDR\_\_SHIFT EQU 000H ; Function Address

FADDR\_UPDATE\_\_BMASK EQU 080H ; Function Address Update

FADDR\_UPDATE\_\_SHIFT EQU 007H ; Function Address Update

FADDR\_UPDATE\_\_NOT\_SET EQU 000H ; The last address written to FADDR is in effect.

FADDR\_UPDATE\_\_SET EQU 080H ; The last address written to FADDR is not yet in

; effect.

;------------------------------------------------------------------------------

; FIFO0 Enums (USB0 Endpoint 0 FIFO Access @ 0x20)

;------------------------------------------------------------------------------

FIFO0\_FIFODATA\_\_FMASK EQU 0FFH ; Endpoint 0 FIFO Access

FIFO0\_FIFODATA\_\_SHIFT EQU 000H ; Endpoint 0 FIFO Access

;------------------------------------------------------------------------------

; FIFO1 Enums (USB0 Endpoint 1 FIFO Access @ 0x21)

;------------------------------------------------------------------------------

FIFO1\_FIFODATA\_\_FMASK EQU 0FFH ; Endpoint 1 FIFO Access

FIFO1\_FIFODATA\_\_SHIFT EQU 000H ; Endpoint 1 FIFO Access

;------------------------------------------------------------------------------

; FIFO2 Enums (USB0 Endpoint 2 FIFO Access @ 0x22)

;------------------------------------------------------------------------------

FIFO2\_FIFODATA\_\_FMASK EQU 0FFH ; Endpoint 2 FIFO Access

FIFO2\_FIFODATA\_\_SHIFT EQU 000H ; Endpoint 2 FIFO Access

;------------------------------------------------------------------------------

; FIFO3 Enums (USB0 Endpoint 3 FIFO Access @ 0x23)

;------------------------------------------------------------------------------

FIFO3\_FIFODATA\_\_FMASK EQU 0FFH ; Endpoint 3 FIFO Access

FIFO3\_FIFODATA\_\_SHIFT EQU 000H ; Endpoint 3 FIFO Access

;------------------------------------------------------------------------------

; FRAMEH Enums (USB0 Frame Number High @ 0x0D)

;------------------------------------------------------------------------------

FRAMEH\_FRMEH\_\_FMASK EQU 007H ; Frame Number High

FRAMEH\_FRMEH\_\_SHIFT EQU 000H ; Frame Number High

;------------------------------------------------------------------------------

; FRAMEL Enums (USB0 Frame Number Low @ 0x0C)

;------------------------------------------------------------------------------

FRAMEL\_FRMEL\_\_FMASK EQU 0FFH ; Frame Number Low

FRAMEL\_FRMEL\_\_SHIFT EQU 000H ; Frame Number Low

;------------------------------------------------------------------------------

; IN1IE Enums (USB0 IN Endpoint Interrupt Enable @ 0x07)

;------------------------------------------------------------------------------

IN1IE\_EP0E\_\_BMASK EQU 001H ; Endpoint 0 Interrupt Enable

IN1IE\_EP0E\_\_SHIFT EQU 000H ; Endpoint 0 Interrupt Enable

IN1IE\_EP0E\_\_DISABLED EQU 000H ; Disable Endpoint 0 interrupts.

IN1IE\_EP0E\_\_ENABLED EQU 001H ; Enable Endpoint 0 interrupts.

IN1IE\_IN1E\_\_BMASK EQU 002H ; IN Endpoint 1 Interrupt Enable

IN1IE\_IN1E\_\_SHIFT EQU 001H ; IN Endpoint 1 Interrupt Enable

IN1IE\_IN1E\_\_DISABLED EQU 000H ; Disable Endpoint 1 IN interrupts.

IN1IE\_IN1E\_\_ENABLED EQU 002H ; Enable Endpoint 1 IN interrupts.

IN1IE\_IN2E\_\_BMASK EQU 004H ; IN Endpoint 2 Interrupt Enable

IN1IE\_IN2E\_\_SHIFT EQU 002H ; IN Endpoint 2 Interrupt Enable

IN1IE\_IN2E\_\_DISABLED EQU 000H ; Disable Endpoint 2 IN interrupts.

IN1IE\_IN2E\_\_ENABLED EQU 004H ; Enable Endpoint 2 IN interrupts.

IN1IE\_IN3E\_\_BMASK EQU 008H ; IN Endpoint 3 Interrupt Enable

IN1IE\_IN3E\_\_SHIFT EQU 003H ; IN Endpoint 3 Interrupt Enable

IN1IE\_IN3E\_\_DISABLED EQU 000H ; Disable Endpoint 3 IN interrupts.

IN1IE\_IN3E\_\_ENABLED EQU 008H ; Enable Endpoint 3 IN interrupts.

;------------------------------------------------------------------------------

; IN1INT Enums (USB0 IN Endpoint Interrupt @ 0x02)

;------------------------------------------------------------------------------

IN1INT\_EP0\_\_BMASK EQU 001H ; Endpoint 0 Interrupt Flag

IN1INT\_EP0\_\_SHIFT EQU 000H ; Endpoint 0 Interrupt Flag

IN1INT\_EP0\_\_NOT\_SET EQU 000H ; Endpoint 0 interrupt inactive.

IN1INT\_EP0\_\_SET EQU 001H ; Endpoint 0 interrupt active.

IN1INT\_IN1\_\_BMASK EQU 002H ; IN Endpoint 1 Interrupt Flag

IN1INT\_IN1\_\_SHIFT EQU 001H ; IN Endpoint 1 Interrupt Flag

IN1INT\_IN1\_\_NOT\_SET EQU 000H ; IN Endpoint 1 interrupt inactive.

IN1INT\_IN1\_\_SET EQU 002H ; IN Endpoint 1 interrupt active.

IN1INT\_IN2\_\_BMASK EQU 004H ; IN Endpoint 2 Interrupt Flag

IN1INT\_IN2\_\_SHIFT EQU 002H ; IN Endpoint 2 Interrupt Flag

IN1INT\_IN2\_\_NOT\_SET EQU 000H ; IN Endpoint 2 interrupt inactive.

IN1INT\_IN2\_\_SET EQU 004H ; IN Endpoint 2 interrupt active.

IN1INT\_IN3\_\_BMASK EQU 008H ; IN Endpoint 3 Interrupt Flag

IN1INT\_IN3\_\_SHIFT EQU 003H ; IN Endpoint 3 Interrupt Flag

IN1INT\_IN3\_\_NOT\_SET EQU 000H ; IN Endpoint 3 interrupt inactive.

IN1INT\_IN3\_\_SET EQU 008H ; IN Endpoint 3 interrupt active.

;------------------------------------------------------------------------------

; INDEX Enums (USB0 Endpoint Index @ 0x0E)

;------------------------------------------------------------------------------

INDEX\_EPSEL\_\_FMASK EQU 00FH ; Endpoint Select Bits

INDEX\_EPSEL\_\_SHIFT EQU 000H ; Endpoint Select Bits

INDEX\_EPSEL\_\_ENDPOINT\_0 EQU 000H ; Endpoint 0.

INDEX\_EPSEL\_\_ENDPOINT\_1 EQU 001H ; Endpoint 1.

INDEX\_EPSEL\_\_ENDPOINT\_2 EQU 002H ; Endpoint 2.

INDEX\_EPSEL\_\_ENDPOINT\_3 EQU 003H ; Endpoint 3.

;------------------------------------------------------------------------------

; OUT1IE Enums (USB0 OUT Endpoint Interrupt Enable @ 0x09)

;------------------------------------------------------------------------------

OUT1IE\_OUT1E\_\_BMASK EQU 002H ; OUT Endpoint 1 Interrupt Enable

OUT1IE\_OUT1E\_\_SHIFT EQU 001H ; OUT Endpoint 1 Interrupt Enable

OUT1IE\_OUT1E\_\_DISABLED EQU 000H ; Disable Endpoint 1 OUT interrupts.

OUT1IE\_OUT1E\_\_ENABLED EQU 002H ; Enable Endpoint 1 OUT interrupts.

OUT1IE\_OUT2E\_\_BMASK EQU 004H ; OUT Endpoint 2 Interrupt Enable

OUT1IE\_OUT2E\_\_SHIFT EQU 002H ; OUT Endpoint 2 Interrupt Enable

OUT1IE\_OUT2E\_\_DISABLED EQU 000H ; Disable Endpoint 2 OUT interrupts.

OUT1IE\_OUT2E\_\_ENABLED EQU 004H ; Enable Endpoint 2 OUT interrupts.

OUT1IE\_OUT3E\_\_BMASK EQU 008H ; OUT Endpoint 3 Interrupt Enable

OUT1IE\_OUT3E\_\_SHIFT EQU 003H ; OUT Endpoint 3 Interrupt Enable

OUT1IE\_OUT3E\_\_DISABLED EQU 000H ; Disable Endpoint 3 OUT interrupts.

OUT1IE\_OUT3E\_\_ENABLED EQU 008H ; Enable Endpoint 3 OUT interrupts.

;------------------------------------------------------------------------------

; OUT1INT Enums (USB0 OUT Endpoint Interrupt @ 0x04)

;------------------------------------------------------------------------------

OUT1INT\_OUT1\_\_BMASK EQU 002H ; OUT Endpoint 1 Interrupt Flag

OUT1INT\_OUT1\_\_SHIFT EQU 001H ; OUT Endpoint 1 Interrupt Flag

OUT1INT\_OUT1\_\_NOT\_SET EQU 000H ; OUT Endpoint 1 interrupt inactive.

OUT1INT\_OUT1\_\_SET EQU 002H ; OUT Endpoint 1 interrupt active.

OUT1INT\_OUT2\_\_BMASK EQU 004H ; OUT Endpoint 2 Interrupt Flag

OUT1INT\_OUT2\_\_SHIFT EQU 002H ; OUT Endpoint 2 Interrupt Flag

OUT1INT\_OUT2\_\_NOT\_SET EQU 000H ; OUT Endpoint 2 interrupt inactive.

OUT1INT\_OUT2\_\_SET EQU 004H ; OUT Endpoint 2 interrupt active.

OUT1INT\_OUT3\_\_BMASK EQU 008H ; OUT Endpoint 3 Interrupt Flag

OUT1INT\_OUT3\_\_SHIFT EQU 003H ; OUT Endpoint 3 Interrupt Flag

OUT1INT\_OUT3\_\_NOT\_SET EQU 000H ; OUT Endpoint 3 interrupt inactive.

OUT1INT\_OUT3\_\_SET EQU 008H ; OUT Endpoint 3 interrupt active.

;------------------------------------------------------------------------------

; POWER Enums (USB0 Power @ 0x01)

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POWER\_SUSEN\_\_BMASK EQU 001H ; Suspend Detection Enable

POWER\_SUSEN\_\_SHIFT EQU 000H ; Suspend Detection Enable

POWER\_SUSEN\_\_DISABLED EQU 000H ; Disable suspend detection. USB0 will ignore

; suspend signaling on the bus.

POWER\_SUSEN\_\_ENABLED EQU 001H ; Enable suspend detection. USB0 will enter suspend

; mode if it detects suspend signaling on the bus.

POWER\_SUSMD\_\_BMASK EQU 002H ; Suspend Mode

POWER\_SUSMD\_\_SHIFT EQU 001H ; Suspend Mode

POWER\_SUSMD\_\_NOT\_SUSPENDED EQU 000H ; USB0 not in suspend mode.

POWER\_SUSMD\_\_SUSPENDED EQU 002H ; USB0 in suspend mode.

POWER\_RESUME\_\_BMASK EQU 004H ; Force Resume

POWER\_RESUME\_\_SHIFT EQU 002H ; Force Resume

POWER\_RESUME\_\_START EQU 004H ; Generate resume signalling to create a remote

; wakeup event.

POWER\_USBRST\_\_BMASK EQU 008H ; Reset Detect

POWER\_USBRST\_\_SHIFT EQU 003H ; Reset Detect

POWER\_USBRST\_\_NOT\_SET EQU 000H ; USB reset signalling not detected.

POWER\_USBRST\_\_SET EQU 008H ; USB reset signalling detected.

POWER\_USBINH\_\_BMASK EQU 010H ; USB0 Inhibit

POWER\_USBINH\_\_SHIFT EQU 004H ; USB0 Inhibit

POWER\_USBINH\_\_ENABLED EQU 000H ; USB0 enabled.

POWER\_USBINH\_\_DISABLED EQU 010H ; USB0 inhibited. All USB traffic is ignored.

POWER\_ISOUD\_\_BMASK EQU 080H ; Isochronous Update Mode

POWER\_ISOUD\_\_SHIFT EQU 007H ; Isochronous Update Mode

POWER\_ISOUD\_\_IN\_TOKEN EQU 000H ; When firmware writes INPRDY = 1, USB0 will send

; the packet when the next IN token is received.

POWER\_ISOUD\_\_SOF\_TOKEN EQU 080H ; When firmware writes INPRDY = 1, USB0 will wait

; for a SOF token before sending the packet. If an

; IN token is received before a SOF token, USB0 will

; send a zero-length data packet.

;------------------------------------------------------------------------------

; USB0ADR Enums (USB0 Indirect Address @ 0x96)

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USB0ADR\_USB0ADR\_\_FMASK EQU 03FH ; USB0 Indirect Register Address

USB0ADR\_USB0ADR\_\_SHIFT EQU 000H ; USB0 Indirect Register Address

USB0ADR\_USB0ADR\_\_FADDR EQU 000H ; Function Address.

USB0ADR\_USB0ADR\_\_POWER EQU 001H ; Power Management.

USB0ADR\_USB0ADR\_\_IN1INT EQU 002H ; Endpoint 0 and Endpoints 1-3 IN Interrupt Flags.

USB0ADR\_USB0ADR\_\_OUT1INT EQU 004H ; Endpoints 1-3 OUT Interrupt Flags.

USB0ADR\_USB0ADR\_\_CMINT EQU 006H ; Common USB Interrupt Flags.

USB0ADR\_USB0ADR\_\_IN1IE EQU 007H ; Endpoint 0 and Endpoints 1-3 IN Interrupt Enables.

USB0ADR\_USB0ADR\_\_OUT1IE EQU 009H ; Endpoints 1-3 OUT Interrupt Enables.

USB0ADR\_USB0ADR\_\_CMIE EQU 00BH ; Common USB Interrupt Enables.

USB0ADR\_USB0ADR\_\_FRAMEL EQU 00CH ; Frame Number Low Byte.

USB0ADR\_USB0ADR\_\_FRAMEH EQU 00DH ; Frame Number High Byte.

USB0ADR\_USB0ADR\_\_INDEX EQU 00EH ; Endpoint Index Selection.

USB0ADR\_USB0ADR\_\_CLKREC EQU 00FH ; Clock Recovery Control.

USB0ADR\_USB0ADR\_\_E0CSR\_EINCSRL EQU 011H ; Endpoint 0 Control / Status, Endpoint IN Control /

; Status Low Byte.

USB0ADR\_USB0ADR\_\_EINCSRH EQU 012H ; Endpoint IN Control / Status High Byte.

USB0ADR\_USB0ADR\_\_EOUTCSRL EQU 014H ; Endpoint OUT Control / Status Low Byte.

USB0ADR\_USB0ADR\_\_EOUTCSRH EQU 015H ; Endpoint OUT Control / Status High Byte.

USB0ADR\_USB0ADR\_\_E0CNT\_EOUTCNTL EQU 016H ; Number of Received Bytes in Endpoint 0 FIFO,

; Endpoint OUT Packet Count Low Byte.

USB0ADR\_USB0ADR\_\_EOUTCNTH EQU 017H ; Endpoint OUT Packet Count High Byte.

USB0ADR\_USB0ADR\_\_EENABLE EQU 01EH ; Endpoint Enable.

USB0ADR\_USB0ADR\_\_FIFO0 EQU 020H ; Endpoint 0 FIFO.

USB0ADR\_USB0ADR\_\_FIFO1 EQU 021H ; Endpoint 1 FIFO.

USB0ADR\_USB0ADR\_\_FIFO2 EQU 022H ; Endpoint 2 FIFO.

USB0ADR\_USB0ADR\_\_FIFO3 EQU 023H ; Endpoint 3 FIFO.

USB0ADR\_AUTORD\_\_BMASK EQU 040H ; USB0 Register Auto-Read Flag

USB0ADR\_AUTORD\_\_SHIFT EQU 006H ; USB0 Register Auto-Read Flag

USB0ADR\_AUTORD\_\_DISABLED EQU 000H ; BUSY must be written manually for each USB0

; indirect register read.

USB0ADR\_AUTORD\_\_ENABLED EQU 040H ; The next indirect register read will automatically

; be initiated when firmware reads USB0DAT (USBADDR

; bits will not be changed).

USB0ADR\_BUSY\_\_BMASK EQU 080H ; USB0 Register Read Busy Flag

USB0ADR\_BUSY\_\_SHIFT EQU 007H ; USB0 Register Read Busy Flag

USB0ADR\_BUSY\_\_NOT\_SET EQU 000H ; A read is not in progress.

USB0ADR\_BUSY\_\_SET EQU 080H ; Initiate a read or a read is in progress.

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; USB0DAT Enums (USB0 Data @ 0x97)

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USB0DAT\_USB0DAT\_\_FMASK EQU 0FFH ; USB0 Data

USB0DAT\_USB0DAT\_\_SHIFT EQU 000H ; USB0 Data

;------------------------------------------------------------------------------

; USB0XCN Enums (USB0 Transceiver Control @ 0xD7)

;------------------------------------------------------------------------------

USB0XCN\_Dn\_\_BMASK EQU 001H ; D- Signal Status

USB0XCN\_Dn\_\_SHIFT EQU 000H ; D- Signal Status

USB0XCN\_Dn\_\_LOW EQU 000H ; D- signal currently at logic 0.

USB0XCN\_Dn\_\_HIGH EQU 001H ; D- signal currently at logic 1.

USB0XCN\_Dp\_\_BMASK EQU 002H ; D+ Signal Status

USB0XCN\_Dp\_\_SHIFT EQU 001H ; D+ Signal Status

USB0XCN\_Dp\_\_LOW EQU 000H ; D+ signal currently at logic 0.

USB0XCN\_Dp\_\_HIGH EQU 002H ; D+ signal currently at logic 1.

USB0XCN\_DFREC\_\_BMASK EQU 004H ; Differential Receiver

USB0XCN\_DFREC\_\_SHIFT EQU 002H ; Differential Receiver

USB0XCN\_DFREC\_\_DIFFERENTIAL\_ZERO EQU 000H ; Differential 0 signalling on the bus.

USB0XCN\_DFREC\_\_DIFFERENTIAL\_ONE EQU 004H ; Differential 1 signalling on the bus.

USB0XCN\_PHYTST\_\_FMASK EQU 018H ; Physical Layer Test

USB0XCN\_PHYTST\_\_SHIFT EQU 003H ; Physical Layer Test

USB0XCN\_PHYTST\_\_MODE0 EQU 000H ; Mode 0: Normal (non-test mode) (D+ = X, D- = X).

USB0XCN\_PHYTST\_\_MODE1 EQU 008H ; Mode 1: Differential 1 forced (D+ = 1, D- = 0).

USB0XCN\_PHYTST\_\_MODE2 EQU 010H ; Mode 2: Differential 0 forced (D+ = 0, D- = 1).

USB0XCN\_PHYTST\_\_MODE3 EQU 018H ; Mode 3: Single-Ended 0 forced (D+ = 0, D- = 0).

USB0XCN\_SPEED\_\_BMASK EQU 020H ; USB0 Speed Select

USB0XCN\_SPEED\_\_SHIFT EQU 005H ; USB0 Speed Select

USB0XCN\_SPEED\_\_LOW\_SPEED EQU 000H ; USB0 operates as a Low Speed device. If enabled,

; the internal pull-up resistor appears on the D-

; line.

USB0XCN\_SPEED\_\_FULL\_SPEED EQU 020H ; USB0 operates as a Full Speed device. If enabled,

; the internal pull-up resistor appears on the D+

; line.

USB0XCN\_PHYEN\_\_BMASK EQU 040H ; Physical Layer Enable

USB0XCN\_PHYEN\_\_SHIFT EQU 006H ; Physical Layer Enable

USB0XCN\_PHYEN\_\_DISABLED EQU 000H ; Disable the USB0 physical layer transceiver

; (suspend).

USB0XCN\_PHYEN\_\_ENABLED EQU 040H ; Enable the USB0 physical layer transceiver

; (normal).

USB0XCN\_PREN\_\_BMASK EQU 080H ; Internal Pull-up Resistor Enable

USB0XCN\_PREN\_\_SHIFT EQU 007H ; Internal Pull-up Resistor Enable

USB0XCN\_PREN\_\_PULL\_UP\_DISABLED EQU 000H ; Internal pull-up resistor disabled (device

; effectively detached from USB network).

USB0XCN\_PREN\_\_PULL\_UP\_ENABLED EQU 080H ; Internal pull-up resistor enabled when VBUS is

; present (device attached to the USB network).

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; VDM0CN Enums (Supply Monitor Control @ 0xFF)

;------------------------------------------------------------------------------

VDM0CN\_VDDSTAT\_\_BMASK EQU 040H ; Supply Status

VDM0CN\_VDDSTAT\_\_SHIFT EQU 006H ; Supply Status

VDM0CN\_VDDSTAT\_\_BELOW EQU 000H ; VDD is at or below the supply monitor threshold.

VDM0CN\_VDDSTAT\_\_ABOVE EQU 040H ; VDD is above the supply monitor threshold.

VDM0CN\_VDMEN\_\_BMASK EQU 080H ; Supply Monitor Enable

VDM0CN\_VDMEN\_\_SHIFT EQU 007H ; Supply Monitor Enable

VDM0CN\_VDMEN\_\_DISABLED EQU 000H ; Supply Monitor Disabled.

VDM0CN\_VDMEN\_\_ENABLED EQU 080H ; Supply Monitor Enabled.

;------------------------------------------------------------------------------

; REF0CN Enums (Voltage Reference Control @ 0xD1)

;------------------------------------------------------------------------------

REF0CN\_REFBE\_\_BMASK EQU 001H ; Internal Reference Buffer Enable

REF0CN\_REFBE\_\_SHIFT EQU 000H ; Internal Reference Buffer Enable

REF0CN\_REFBE\_\_DISABLED EQU 000H ; Disable the internal reference buffer.

REF0CN\_REFBE\_\_ENABLED EQU 001H ; Enable the internal reference buffer. The internal

; voltage reference is driven on the VREF pin.

REF0CN\_TEMPE\_\_BMASK EQU 004H ; Temperature Sensor Enable

REF0CN\_TEMPE\_\_SHIFT EQU 002H ; Temperature Sensor Enable

REF0CN\_TEMPE\_\_DISABLED EQU 000H ; Disable the internal Temperature Sensor.

REF0CN\_TEMPE\_\_ENABLED EQU 004H ; Enable the internal Temperature Sensor.

REF0CN\_REFSL\_\_BMASK EQU 008H ; Voltage Reference Select

REF0CN\_REFSL\_\_SHIFT EQU 003H ; Voltage Reference Select

REF0CN\_REFSL\_\_VREF EQU 000H ; Use the VREF pin as the voltage reference.

REF0CN\_REFSL\_\_VDD EQU 008H ; Use VDD as the voltage reference.

REF0CN\_REGOVR\_\_BMASK EQU 010H ; Regulator Reference Override

REF0CN\_REGOVR\_\_SHIFT EQU 004H ; Regulator Reference Override

REF0CN\_REGOVR\_\_REFSL EQU 000H ; The REFSL bit selects the voltage reference

; source.

REF0CN\_REGOVR\_\_VREG EQU 010H ; Use the output of the internal regulator as the

; voltage reference source.

REF0CN\_REFBGS\_\_BMASK EQU 080H ; Reference Buffer Gain Select

REF0CN\_REFBGS\_\_SHIFT EQU 007H ; Reference Buffer Gain Select

REF0CN\_REFBGS\_\_GAIN\_2 EQU 000H ; The on-chip voltage reference buffer gain is 2.

REF0CN\_REFBGS\_\_GAIN\_1 EQU 080H ; The on-chip voltage reference buffer gain is 1.

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; REG01CN Enums (Voltage Regulator Control @ 0xC9)

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REG01CN\_REG1MD\_\_BMASK EQU 002H ; VREG1 Voltage Regulator Mode

REG01CN\_REG1MD\_\_SHIFT EQU 001H ; VREG1 Voltage Regulator Mode

REG01CN\_REG1MD\_\_NORMAL EQU 000H ; VREG1 Voltage Regulator in normal mode.

REG01CN\_REG1MD\_\_LOW\_POWER EQU 002H ; VREG1 Voltage Regulator in low power mode.

REG01CN\_STOPCF\_\_BMASK EQU 008H ; VREG1 Stop Mode Configuration

REG01CN\_STOPCF\_\_SHIFT EQU 003H ; VREG1 Stop Mode Configuration

REG01CN\_STOPCF\_\_ACTIVE EQU 000H ; VREG1 Regulator is still active in stop mode. Any

; enabled reset source will reset the device.

REG01CN\_STOPCF\_\_SHUTDOWN EQU 008H ; VREG1 Regulator is shut down in stop mode. Only

; the RSTb pin or power cycle can reset the device.

REG01CN\_REG0MD\_\_BMASK EQU 010H ; VREG0 Voltage Regulator Mode

REG01CN\_REG0MD\_\_SHIFT EQU 004H ; VREG0 Voltage Regulator Mode

REG01CN\_REG0MD\_\_NORMAL EQU 000H ; VREG0 Voltage Regulator in normal mode.

REG01CN\_REG0MD\_\_LOW\_POWER EQU 010H ; VREG0 Voltage Regulator in low power mode.

REG01CN\_VBSTAT\_\_BMASK EQU 040H ; VBUS Signal Status

REG01CN\_VBSTAT\_\_SHIFT EQU 006H ; VBUS Signal Status

REG01CN\_VBSTAT\_\_NOT\_SET EQU 000H ; VBUS signal currently absent (device not attached

; to USB network).

REG01CN\_VBSTAT\_\_SET EQU 040H ; VBUS signal currently present (device attached to

; USB network).

REG01CN\_REG0DIS\_\_BMASK EQU 080H ; Voltage Regulator (REG0) Disable

REG01CN\_REG0DIS\_\_SHIFT EQU 007H ; Voltage Regulator (REG0) Disable

REG01CN\_REG0DIS\_\_ENABLED EQU 000H ; Enable the VREG0 Voltage Regulator.

REG01CN\_REG0DIS\_\_DISABLED EQU 080H ; Disable the VREG0 Voltage Regulator.

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; EMI0CF Enums (External Memory Configuration @ 0x85)

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EMI0CF\_EALE\_\_FMASK EQU 003H ; ALE Pulse-Width Select

EMI0CF\_EALE\_\_SHIFT EQU 000H ; ALE Pulse-Width Select

EMI0CF\_EALE\_\_1\_CLOCK EQU 000H ; ALE high and ALE low pulse width = 1 SYSCLK cycle.

EMI0CF\_EALE\_\_2\_CLOCKS EQU 001H ; ALE high and ALE low pulse width = 2 SYSCLK

; cycles.

EMI0CF\_EALE\_\_3\_CLOCKS EQU 002H ; ALE high and ALE low pulse width = 3 SYSCLK

; cycles.

EMI0CF\_EALE\_\_4\_CLOCKS EQU 003H ; ALE high and ALE low pulse width = 4 SYSCLK

; cycles.

EMI0CF\_EMD\_\_FMASK EQU 00CH ; EMIF Operating Mode Select

EMI0CF\_EMD\_\_SHIFT EQU 002H ; EMIF Operating Mode Select

EMI0CF\_EMD\_\_INTERNAL\_ONLY EQU 000H ; Internal Only: MOVX accesses on-chip XRAM only.

; All effective addresses alias to on-chip memory

; space.

EMI0CF\_EMD\_\_SPLIT\_WITHOUT\_BANK\_SELECT EQU 004H ; Split Mode without Bank Select: Accesses below the

; internal XRAM boundary are directed on-chip.

; Accesses above the internal XRAM boundary are

; directed off-chip. 8-bit off-chip MOVX operations

; use the current contents of the Address high port

; latches to resolve the upper address byte. To

; access off chip space, EMI0CN must be set to a

; page that is not contained in the on-chip address

; space.

EMI0CF\_EMD\_\_SPLIT\_WITH\_BANK\_SELECT EQU 008H ; Split Mode with Bank Select: Accesses below the

; internal XRAM boundary are directed on-chip.

; Accesses above the internal XRAM boundary are

; directed off-chip. 8-bit off-chip MOVX operations

; uses the contents of EMI0CN to determine the high-

; byte of the address.

EMI0CF\_EMD\_\_EXTERNAL\_ONLY EQU 00CH ; External Only: MOVX accesses off-chip XRAM only.

; On-chip XRAM is not visible to the core.

EMI0CF\_MUXMD\_\_BMASK EQU 010H ; EMIF Multiplex Mode Select

EMI0CF\_MUXMD\_\_SHIFT EQU 004H ; EMIF Multiplex Mode Select

EMI0CF\_MUXMD\_\_MULTIPLEXED EQU 000H ; EMIF operates in multiplexed address/data mode.

EMI0CF\_MUXMD\_\_NON\_MULTIPLEXED EQU 010H ; EMIF operates in non-multiplexed mode (separate

; address and data pins).

EMI0CF\_USBFAE\_\_BMASK EQU 040H ; USB FIFO Access Enable

EMI0CF\_USBFAE\_\_SHIFT EQU 006H ; USB FIFO Access Enable

EMI0CF\_USBFAE\_\_FIFO\_ACCESS\_DISABLED EQU 000H ; USB FIFO RAM not available through MOVX

; instructions.

EMI0CF\_USBFAE\_\_FIFO\_ACCESS\_ENABLED EQU 040H ; USB FIFO RAM available using MOVX instructions.

; The 1 kB of USB RAM will be mapped in XRAM space

; at addresses 0x0400 to 0x07FF. The USB clock must

; be active and greater than or equal to twice the

; SYSCLK (USBCLK > 2 x SYSCLK) to access this area

; with MOVX instructions.

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; EMI0CN Enums (External Memory Interface Control @ 0xAA)

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EMI0CN\_PGSEL\_\_FMASK EQU 0FFH ; XRAM Page Select

EMI0CN\_PGSEL\_\_SHIFT EQU 000H ; XRAM Page Select

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; EMI0TC Enums (External Memory Timing Control @ 0x84)

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EMI0TC\_AHOLD\_\_FMASK EQU 003H ; EMIF Address Hold Time

EMI0TC\_AHOLD\_\_SHIFT EQU 000H ; EMIF Address Hold Time

EMI0TC\_AHOLD\_\_0\_CLOCKS EQU 000H ; Address hold time = 0 SYSCLK cycles.

EMI0TC\_AHOLD\_\_1\_CLOCK EQU 001H ; Address hold time = 1 SYSCLK cycle.

EMI0TC\_AHOLD\_\_2\_CLOCKS EQU 002H ; Address hold time = 2 SYSCLK cycles.

EMI0TC\_AHOLD\_\_3\_CLOCKS EQU 003H ; Address hold time = 3 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_FMASK EQU 03CH ; EMIF /WR and /RD Pulse-Width Control

EMI0TC\_PWIDTH\_\_SHIFT EQU 002H ; EMIF /WR and /RD Pulse-Width Control

EMI0TC\_PWIDTH\_\_1\_CLOCK EQU 000H ; /WR and /RD pulse width is 1 SYSCLK cycle.

EMI0TC\_PWIDTH\_\_2\_CLOCKS EQU 004H ; /WR and /RD pulse width is 2 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_3\_CLOCKS EQU 008H ; /WR and /RD pulse width is 3 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_4\_CLOCKS EQU 00CH ; /WR and /RD pulse width is 4 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_5\_CLOCKS EQU 010H ; /WR and /RD pulse width is 5 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_6\_CLOCKS EQU 014H ; /WR and /RD pulse width is 6 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_7\_CLOCKS EQU 018H ; /WR and /RD pulse width is 7 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_8\_CLOCKS EQU 01CH ; /WR and /RD pulse width is 8 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_9\_CLOCKS EQU 020H ; /WR and /RD pulse width is 9 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_10\_CLOCKS EQU 024H ; /WR and /RD pulse width is 10 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_11\_CLOCKS EQU 028H ; /WR and /RD pulse width is 11 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_12\_CLOCKS EQU 02CH ; /WR and /RD pulse width is 12 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_13\_CLOCKS EQU 030H ; /WR and /RD pulse width is 13 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_14\_CLOCKS EQU 034H ; /WR and /RD pulse width is 14 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_15\_CLOCKS EQU 038H ; /WR and /RD pulse width is 15 SYSCLK cycles.

EMI0TC\_PWIDTH\_\_16\_CLOCKS EQU 03CH ; /WR and /RD pulse width is 16 SYSCLK cycles.

EMI0TC\_ASETUP\_\_FMASK EQU 0C0H ; EMIF Address Setup Time

EMI0TC\_ASETUP\_\_SHIFT EQU 006H ; EMIF Address Setup Time

EMI0TC\_ASETUP\_\_0\_CLOCKS EQU 000H ; Address setup time = 0 SYSCLK cycles.

EMI0TC\_ASETUP\_\_1\_CLOCK EQU 040H ; Address setup time = 1 SYSCLK cycle.

EMI0TC\_ASETUP\_\_2\_CLOCKS EQU 080H ; Address setup time = 2 SYSCLK cycles.

EMI0TC\_ASETUP\_\_3\_CLOCKS EQU 0C0H ; Address setup time = 3 SYSCLK cycles.